ANALOG ELECTRONICS NOTES

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Analog Electronics Notes, First Edition

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Analog Electronics

* finding RMS value.

eg: $V(t) = V_m \sin \omega t$.

S1) Square : $V(t) \rightarrow V_m^2 \sin^2 \omega t$

S2) Mean : This signal is periodic with $T = 2\pi$.

$$= \frac{1}{T}\int_0^T V_{(t)}^2 \, dt = \frac{1}{2\pi}\int_0^{2\pi} V_m^2 \sin^2 \omega t \, dt$$

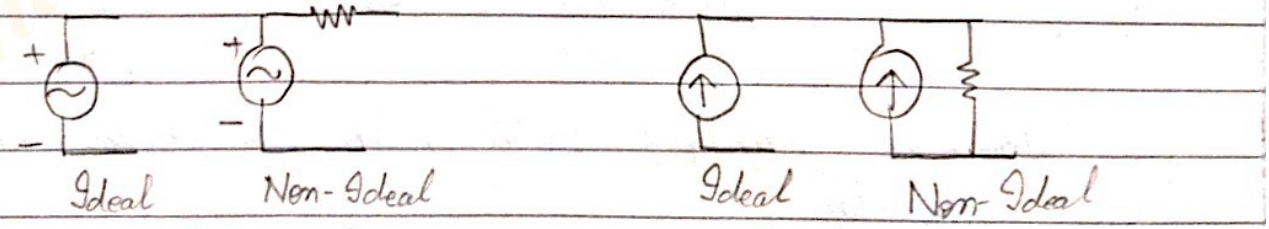
S3) Root :

$$\sqrt{\frac{1}{T}\int_0^T V_{(t)}^2 \, dt} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} V_m^2 \sin^2 \omega t \, dt}$$

*

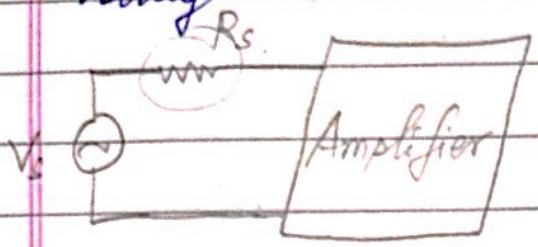
Independent source : Something that can be easily changed without restriction.
(cannot be changed : dependent source)

Independent Voltage & Current Sources



* Independent Source : ◯ ; Dependent Source : ◇

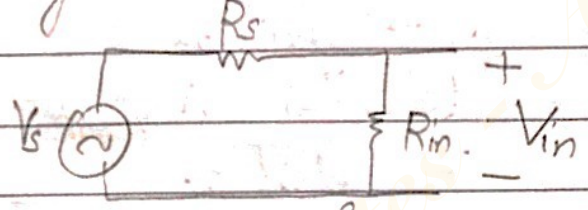
* A non ideal source (found everywhere) is not desirable, as, it reduces the value of source voltage.



Now, we want to reduce the effect of Rs.

Idea : Make the input impedance of amplifier very high.

like :-



By voltage divider rule :

$$V_{in} = \left(\frac{R_{in}}{R_{in} + R_s}\right) V_s$$

$$V_{in} = \left(\frac{1}{1 + \frac{R_s}{R_{in}}}\right) V_s$$

↳ If $R_{in} >> R_s$

$$V_{in} \simeq V_s$$

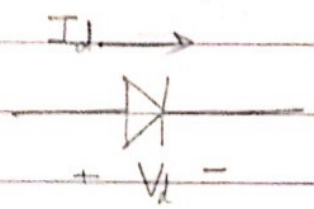
So, Value of source voltage didn't really get reduced.

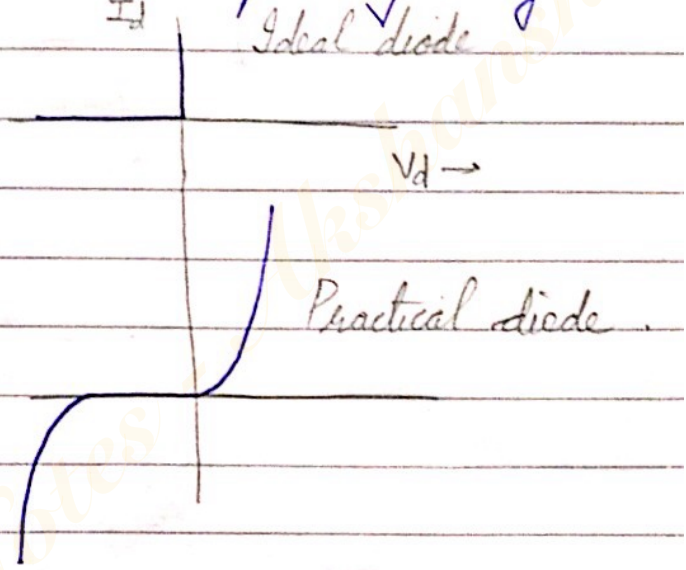
So, an amplifier with high i/p impedance is desirable.

* Note : Revise Norton's theorem, Thévenin's theorem, Max. Power Transfer theorem, Superposition theorem.

✱ DIODES

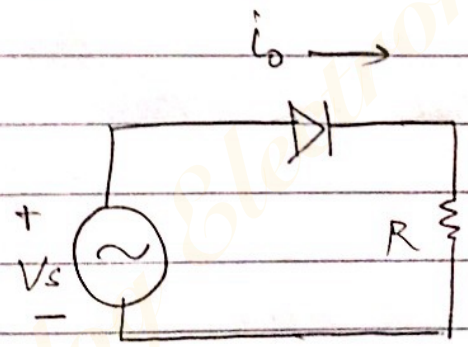
↳ an active device that responds to an i/p voltage and allows current to flow in one dir^{n} for a normal operating range.





✱ Basically, a PN junction diode conducts when FB & (approximately) does not conduct in RB.
Conduct ≡ SC
no Conduct ≡ OC

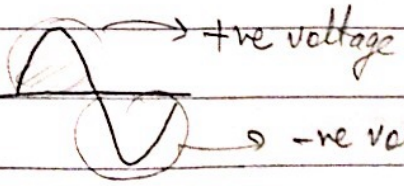
Q.



Assume diode is ideal
If $V_s = V_m \sin \omega t$, identify value(s) of V_o.

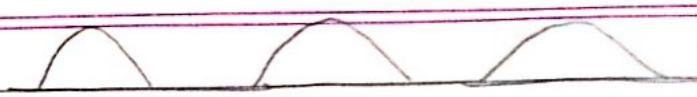
(Idea : For IDEAL diode :-
+ve voltage ⇒ FB → ⟶|⟵ ≡ —•—•— ≡ SC
-ve voltage ⇒ RB → ⟶|⟵ ≡ —• •— ≡ OC)

So, for sine wave i/p



So, for V_s = +ve, $V_o = V_s$
V_s = -ve, $V_o = 0$.

* pd ≡ practical diode

So, V_o = 

behaves as half wave rectifier

Now, using practical diode:

$$i_D = I_s\left(e^{\frac{v_D}{V_T}} - 1\right)$$

↳ for forward bias,

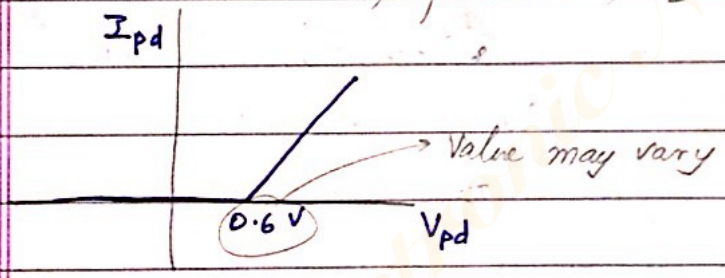
$v_D \simeq 0.7$ & $V_T = 0.026$ (Kmanor)

So, $i_D = I_s\left(e^{\frac{0.7}{0.026}} - 1\right)$

$\approx I_s\left(e^{30} - 1\right)$

$\simeq I_s\left(e^{30}\right)$

So, for FB, $i_D = I_s\left(e^{\frac{v_D}{V_T}}\right)$ (-1 ignored)



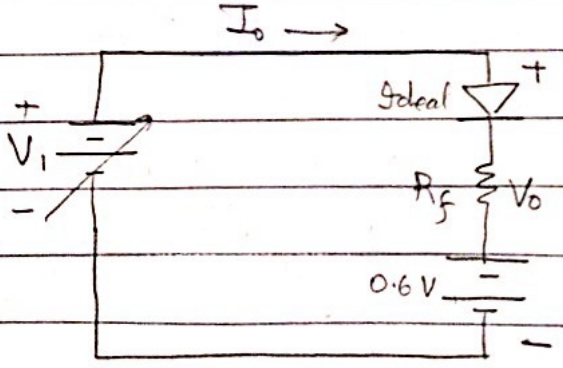
(approximating exponential to linear)

V/I curve a st line

So, basically Ideal diode + 0.6 V + Resistor

=

Practical diode



↳ For this to conduct,

$V_1 \geq 0.6$ V. ≡ V, say

↳ when it conducts, ideal diode = sc. So,

Current across $R_f = \frac{V - 0.6}{R_f}$

Imp. ★ Notation

i_d, v_d : only AC
I_D, V_D : only DC
i_D, v_D : AC & DC

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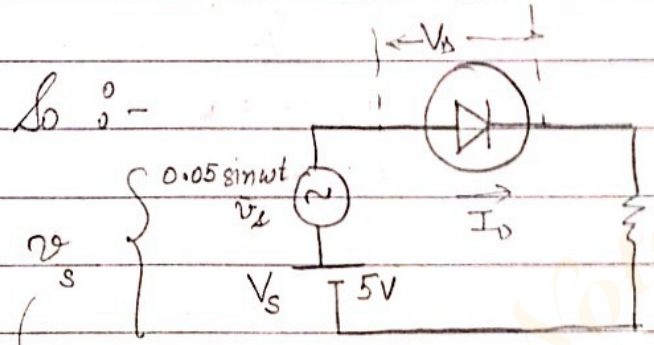
Now, actually, diode's char :

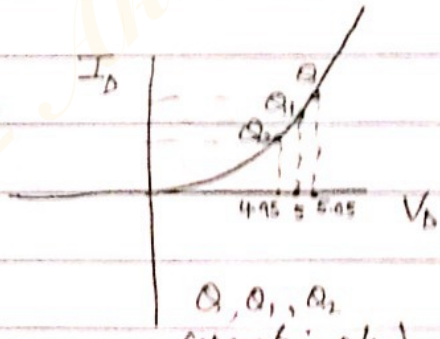
So, to model that,

Idea :

- Use a DC voltage to make diode in OPERATING Region (at operating point, Q).
- Add sine wave over DC.

So :-





Q, Q_1, Q_2 (operating pts.) are on a line.

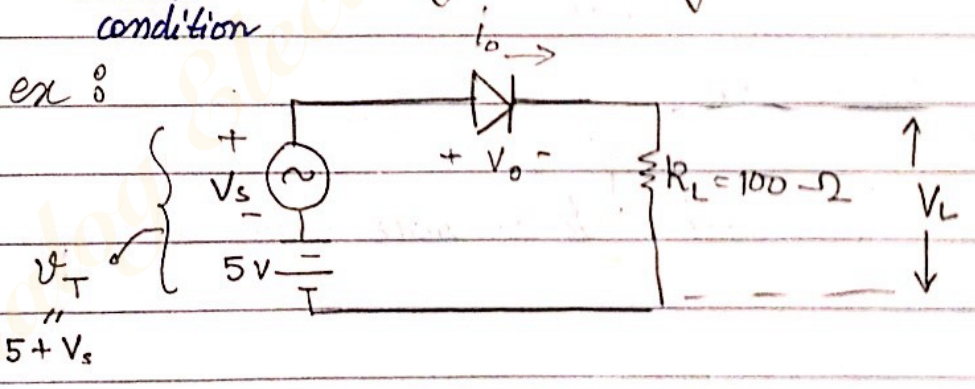
$v_s = v_s + V_S \in (5-0.05, 5+0.05)$

$\in (4.95, 5.05)$

So, diode remains b/w 4.95 to 5.05 V, nearly linear region of char.

when $v_s = V_S$ ($v_s = 0$) → Quiescent condition

ex :



$v_T = V_o + V_L$

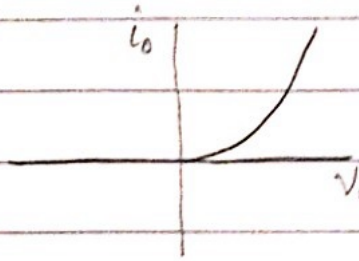
$v_T = V_o + i_o R_L$

$\Rightarrow i_o = (-1/R_L) V_o + (v_T/R_L)$ → (1)

Also, $i_o = I_s (e^{V_o/V_T} - 1)$ → (2)

Solving eqns (1) & (2).

M1 : Graphical method :



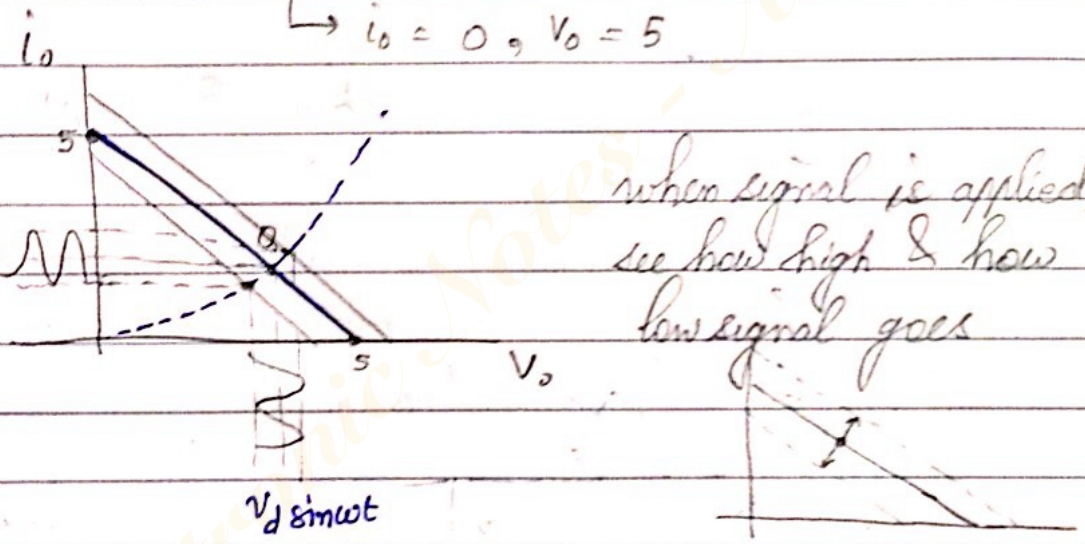
: eqn (2)

Considering quiscent cond^n, $v_T = 5$ (signal not applied)

$\Rightarrow i_0 = (-1/R_L) V_0 + 5/R_L$

$\rightarrow i_0 = 5, V_0 = 0$

$\rightarrow i_0 = 0, V_0 = 5$



when signal is applied, see how high & how low signal goes

- ✓ Ratio of $\frac{V_d \sin\omega t}{i_d \sin\omega t}$ gives diode resistance
- ✓ We can get peak to peak value of current & voltage

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* Parameters than can be used for circuit analysis :
ONLY : Voltage (V), Current (I), Resistor (R), Inductor (L) and Capacitor (C).

✲ Analysis using diode models

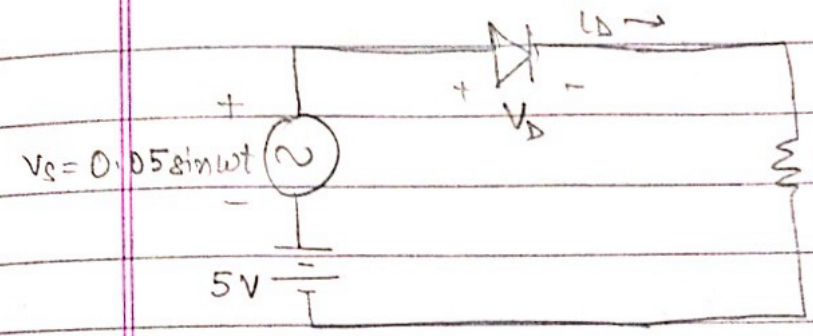
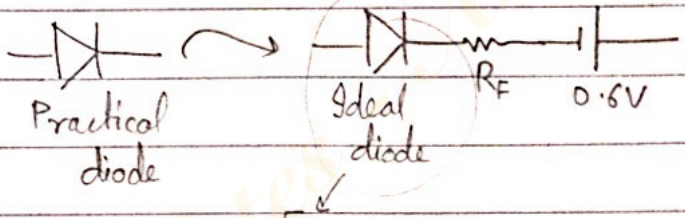
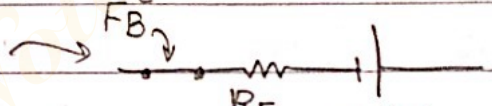


Fig ①

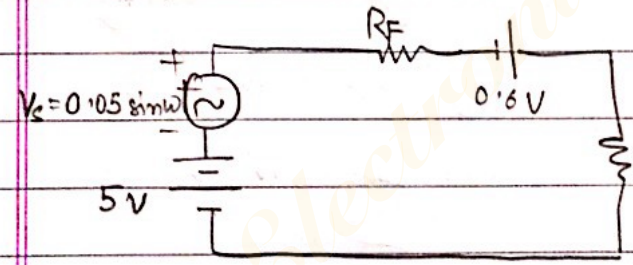
here, i/p voltage is 5 ± 0.05 V. So, diode is always FB

Now,



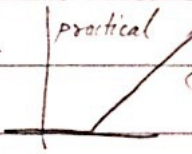


So, diode modelled as :

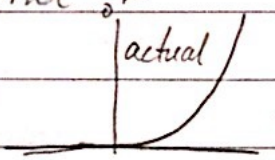


↳ Total i/p, $v_s = 5 + 0.05 \sin \omega t$

Note : we are modelling as :-



not :-



So, finding other way to approximate (i.e, trying to use exponential char

From fig ①

KVL : $V_S = V_D + i_D R_L$ → ①

i.e, $i_D = (v_s - v_D)/R_L$

Also, $i_D = I_S \left[e^{v_D/V_T} - 1 \right]$ → ②

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Solving :-

(M1) Here, we need to separate DC & AC components
i.e. use Superpos^n principle.

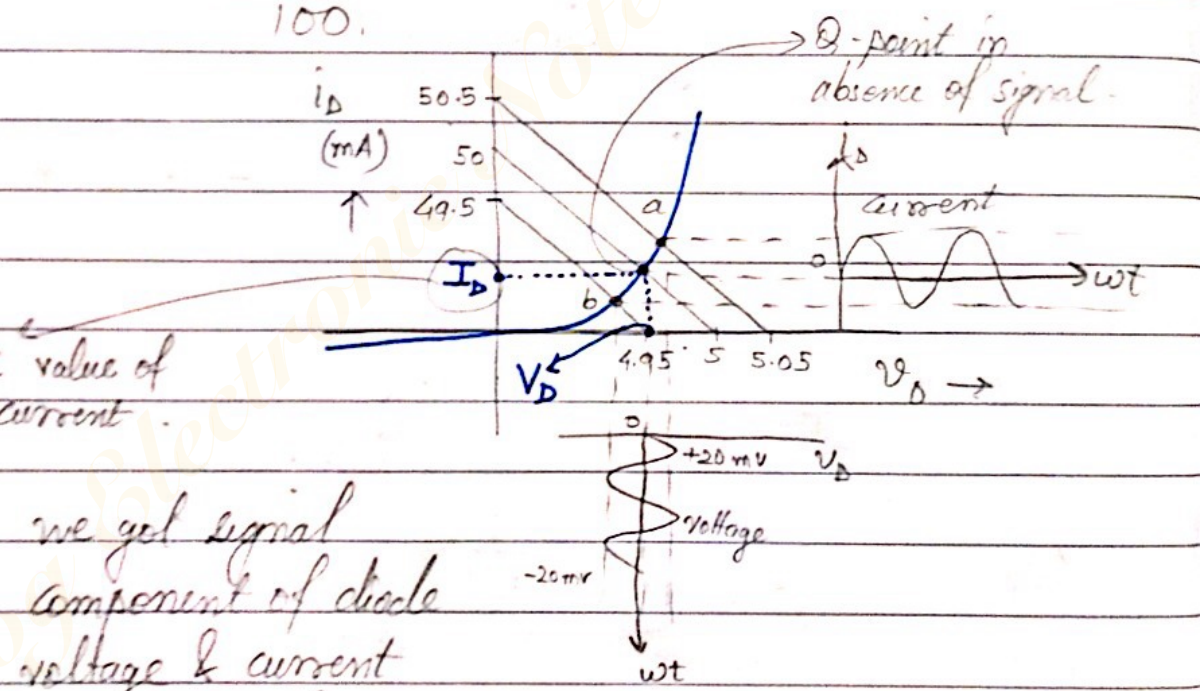
(M2) Keep total values (DC + AC). & use graphical method

Using M2

from eq^n (1), $V_D = 0$, $i_D = 0$

$i_D = \frac{v_s}{R_L}$, $v_D = v_s$

$i_D = \frac{5 \pm 0.05}{100}$ $\qquad$ 5 ± 0.05



we get signal component of diode voltage & current from graphs.

(M1) AC Analysis

Instead using small signal analysis
The signal swing's entire range = 5 ± 0.05 V.
i.e. in this short range, curve can be considered as straight line.

* Note :- $\Delta v_D \equiv v_d$
& $\Delta i_D \equiv i_d$

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For this small range, the diode can be replaced by resistor (r_d) (for Ac component)

So, $\Delta V_D = r_d \Delta i_D$ (or $v_d = r_d i_d$)

Now, finding r_d.

M(a)) Draw graph & find slope at Q-point.

$$r_d = \frac{1}{(\Delta i_D / \Delta V_D)}$$

M(b)) Writing diode eq^n :-

$$i_D = I_S \left[e^{v_D/V_T} - 1 \right] \simeq I_S \left[e^{v_D/V_T} \right]$$

(-1 ignored, $\because$ FB)

For FB, assume $v_D \simeq 0.7\,V$ (usually b/w 0.6 - 0.8 V)

$$\left[\left(e^{\frac{0.6 \text{ or } 0.8}{0.026}} \gg 1 \right), \text{ so, } -1 \text{ ignored} \right]$$

Now, $i_D = I_D + \partial i_D = I_S \left[\underbrace{e^{(V_D/V_T)}}_{I_D} e^{(\partial V_D/V_T)} \right] = I_D e^{\partial V_D/V_T}$

So, $\partial i_D = I_D \left[e^{\partial V_D/V_T} - 1 \right]$

$\partial V_D/V_T$ should be $\ll 1$, so, exponential expansion.

Small signal approxim^n :- $\exp[x] \simeq 1 + x$

$$e^x = 1 + x + \left(\frac{x^2}{2!} + \cdots \right) \rightarrow \text{ignored.}$$

So, $\partial i_D \simeq I_D \left[\frac{\partial V_D}{V_T}\right]$

or $i_d = I_D \frac{v_d}{V_T}$

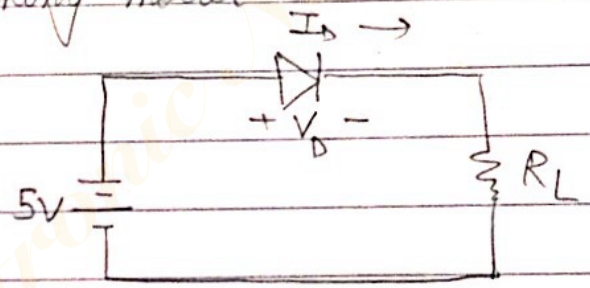
$\Rightarrow v_d = \left(\frac{V_T}{I_D}\right) \times i_d$

Signal component of So, clearly, diode voltage $R_d = \frac{V_T}{I_D}$

Now,

DC Analysis

Finding I_D. Making model :-



$V_S = 5 = V_D + I_D R_L \rightarrow (1)$

& $I_D = I_S \left[e^{V_D/V_T} - 1\right] \rightarrow (2)$

Solving eqns (1) & (2).

M(i) : Graphical method.

M(ii) : Successive approxim^n method.

Using M(ii).

We make assumption on V_D.

Lets say, $V_D = V_{D1} = 0.7\,V$. (usually take this value)

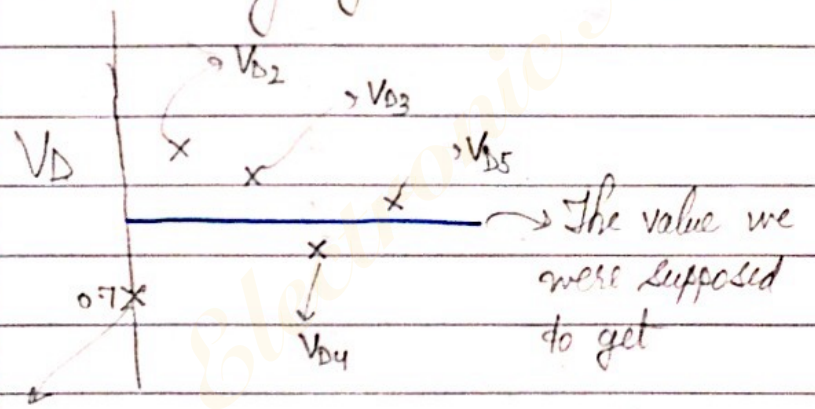
Using V_{D1} in eqn (1)

$$\Rightarrow I_D = \frac{5 - 0.7}{100} = \frac{4.3}{100} = 43\ mA = I_{D1}, \text{ say.}$$

Using I_{D1} in eqn (2), find $V_D = V_{D2}$, say.

Using V_{D2} in eqn (1) again, find $I_D = I_{D2}$, say.

Keep continuing in this manner.
We will get diff^t iterations for V_D & I_D.
Now, analysing iterations.

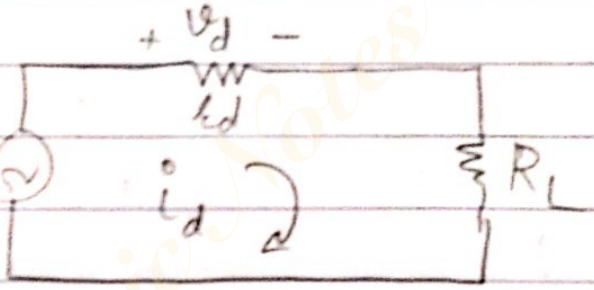


We observe that with iterations increase, we are getting value of V_D close to the actual value that we were supposed to get.

So, stop after 3-4 iterations. We get I_D. Using this I_D, find $r_d = \frac{V_T}{I_D}$.

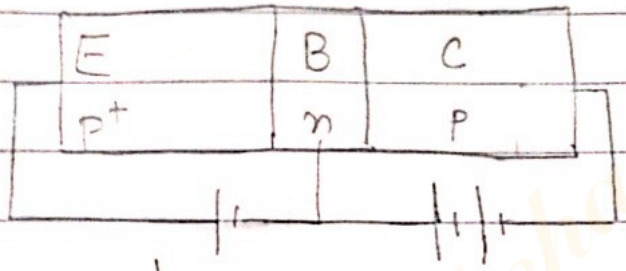
Hence, from the AC analysis, the circuit will be :-

final Ans :-



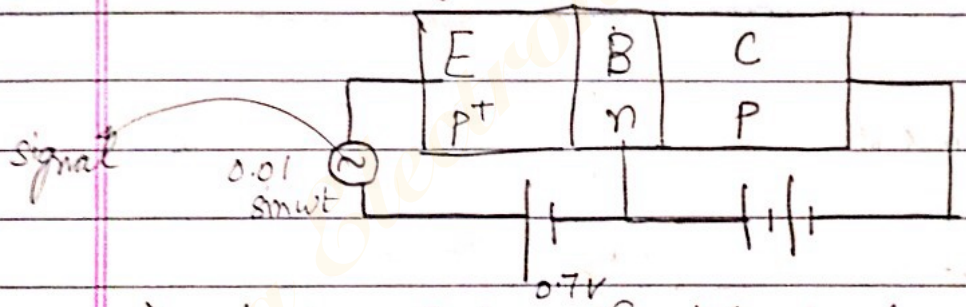
☆ MODELLING A TRANSISTOR.

Basic pnp transistor



→ BJT in active region
(EB Junction → FB
CB Junction → RB)
→ here (pnp transistor), holes are the main carries
→ Size (widths): B << E < C

Applying AC signal on E-side

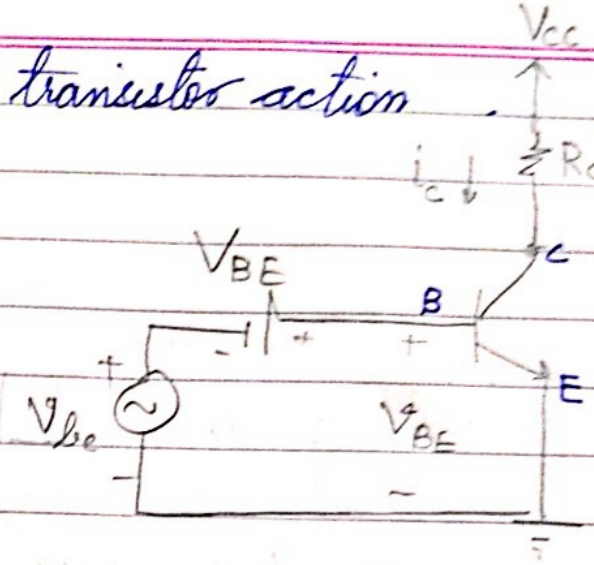


Due to AC signal, the i/p signal voltage varies as $0.7 \pm 0.01V$. So, o/p is also reflected as $0.7 \pm 0.01V$

Idea :-

At o/p we get signal component + DC.
Now, to get signal out of it, use a capacitor.
It filters out DC leaving signal.

- Simple transistor action.



Now

treat a PNP transistor as 2 diodes.

diode 1 diode 2.

i_E, v_{BE} i_C, v_{BC}.

For diode 1, we have characteristic curve of a diode, as done before. i_E vs v_{BE} & $i_E \simeq i_C$.

So, we use,

$$i_C = I_S [e^{v_{BE}/V_T} - 1] \simeq I_S e^{v_{BE}/V_T}$$

Now, $I_C + i_c = I_S e^{V_{BE}/V_T} e^{v_{be}/V_T}$

$$= I_C e^{v_{be}/V_T}$$

$$\Rightarrow i_C = I_C [e^{v_{be}/V_T} - 1]$$

(Just like done before)

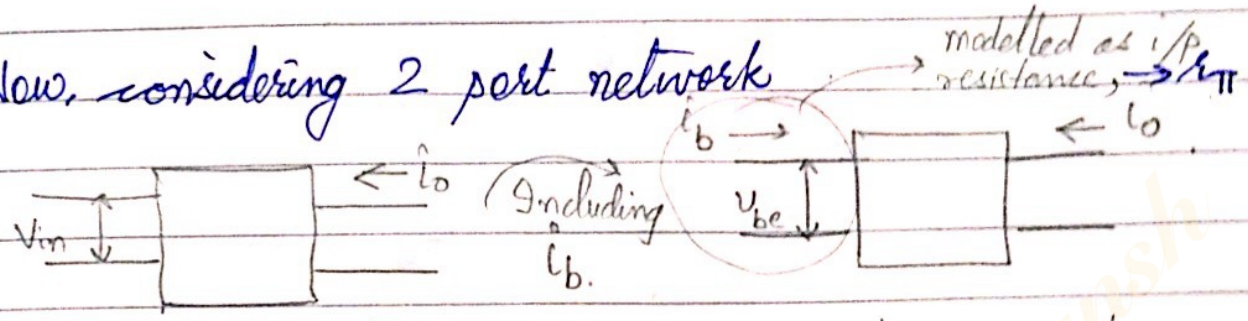
Again, for small signal approxim^n,

$$e^{v_{be}/V_T} = 1 + \frac{v_{be}}{V_T}.$$

$$\Rightarrow i_C \simeq I_C \left[\frac{v_{be}}{V_T}\right]$$

or $\frac{i_c}{v_{be}} = \frac{I_c}{V_T}$

* Now, considering 2 port network

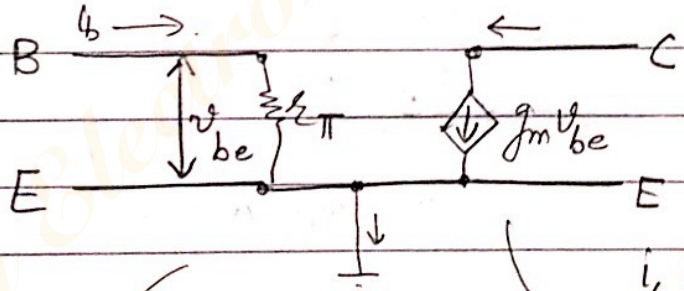


$\frac{i_o}{V_{in}}$ = transconductance or AC transconductance, g_m.

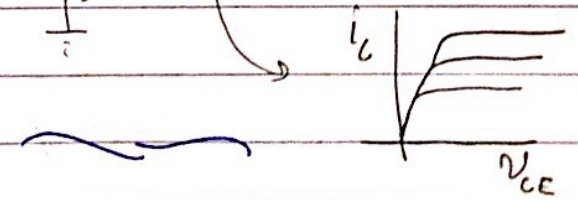
So, $i_c = \left(\frac{I_c}{V_T}\right) v_{be} = g_m v_{be}$

→ Input BE voltage has a linear relnship with o/p current. & the linear factor is g_m.

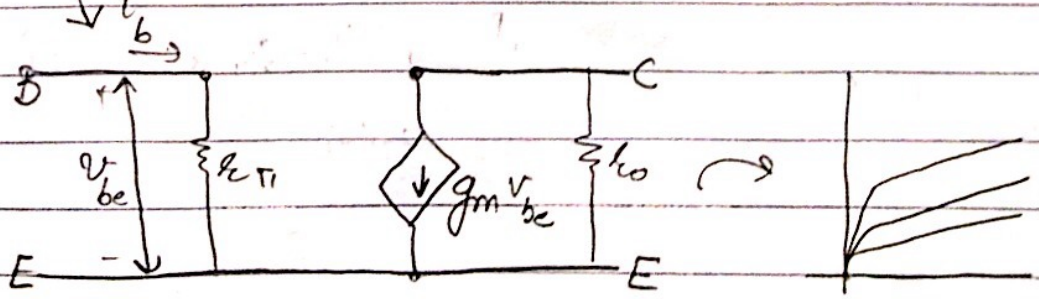
So, we have:

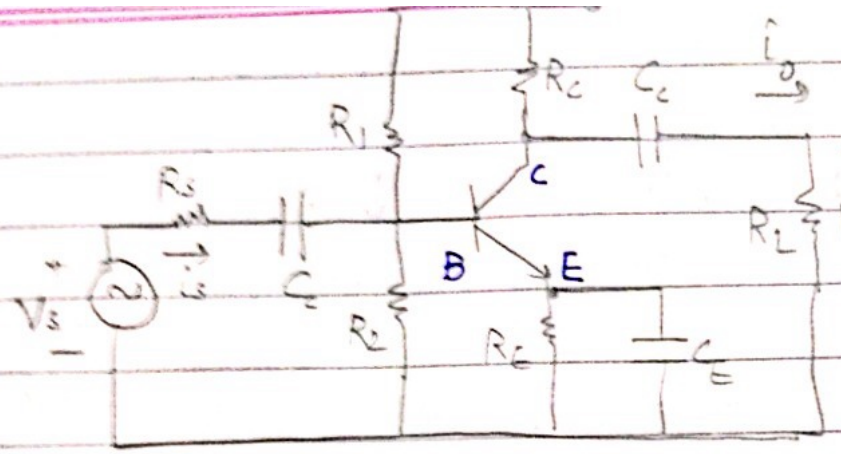


: Small signal model of transistor



for practical BJT





CE Amplifier (Std. circuit)

Now, drawing small signal circuit

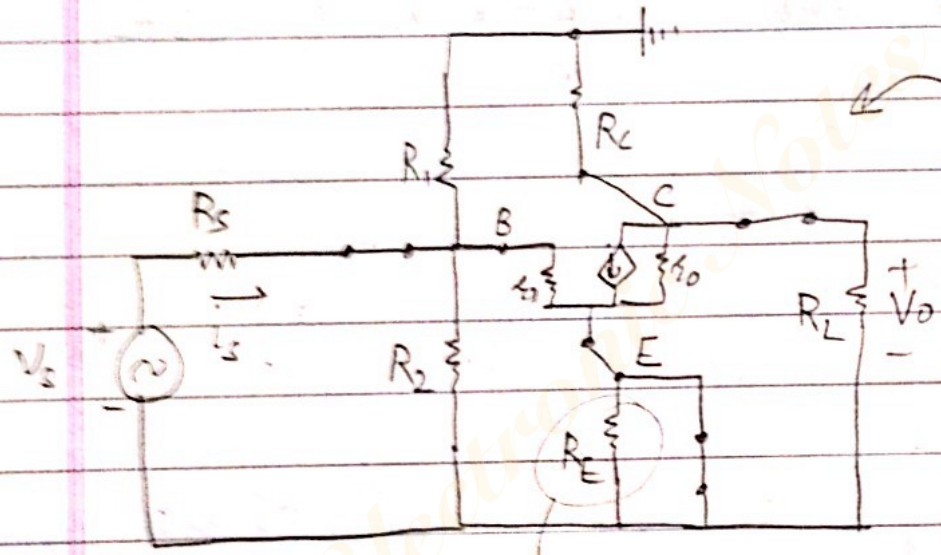
⇓

only signal ⇒ only AC, no DC

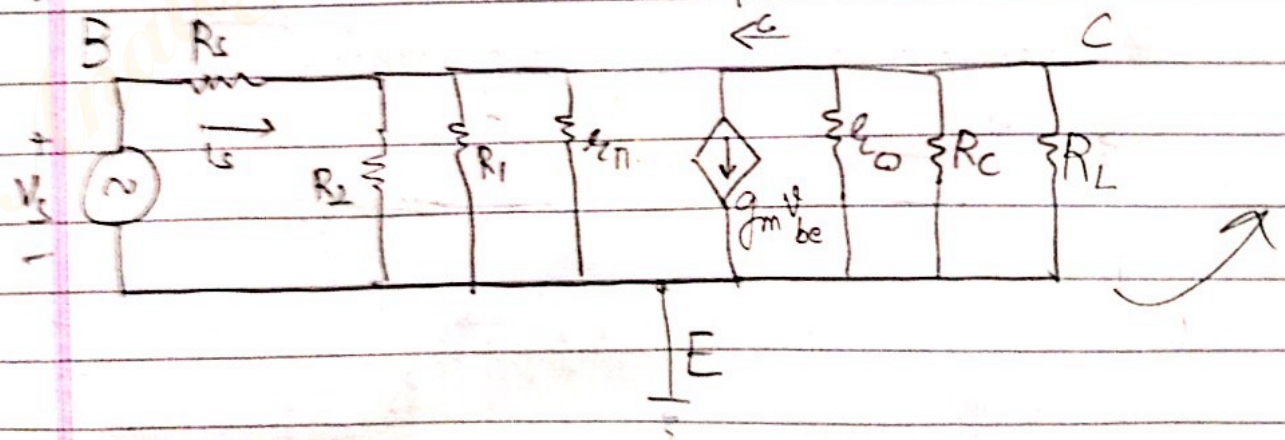
⇓

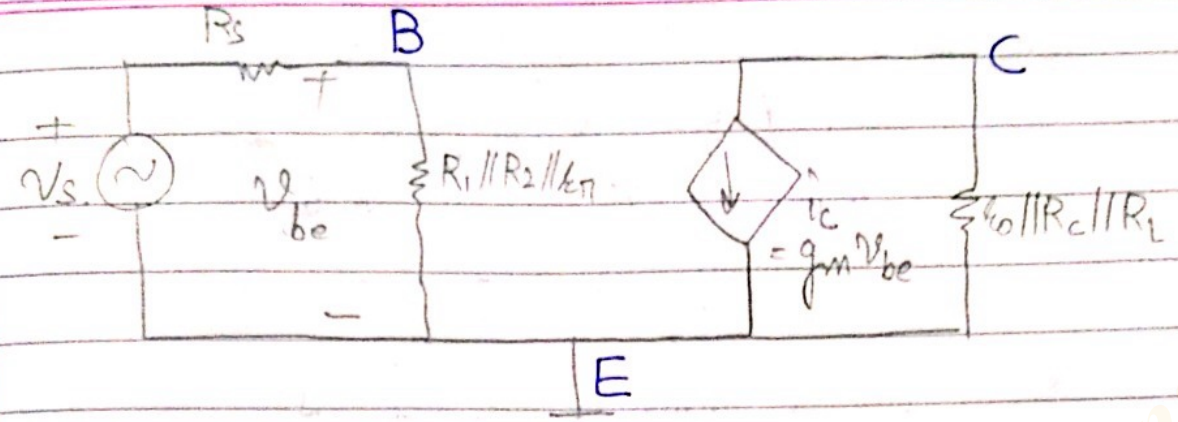
Remove / ground all DC.

- Voltage → ground
- Capacitors → SC
- Replace transistor with model



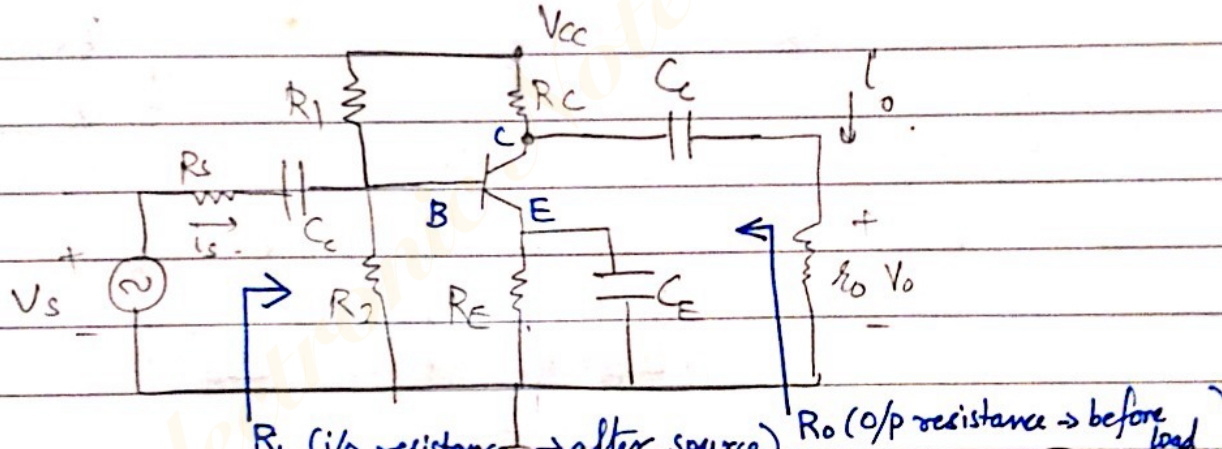
This Resistance is bypassed by a SC



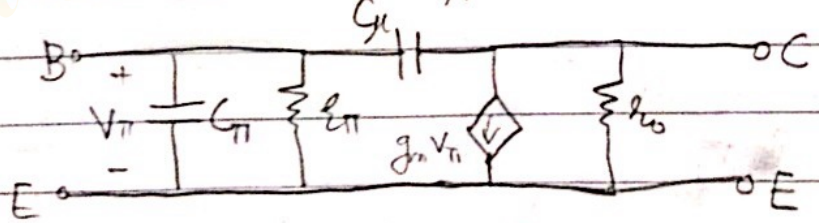


(final model of a BJT → small signal)

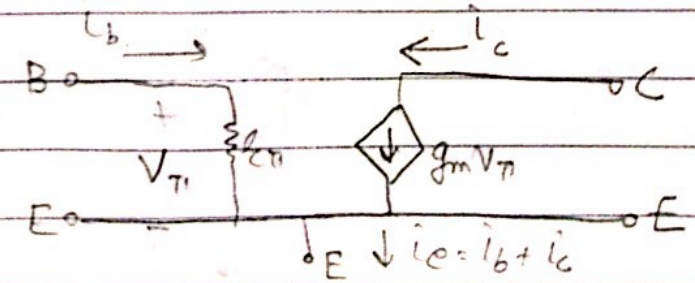
eg: $V_{CC} = 15V$, $R_s = 1k\Omega$, $R_1 = 60k\Omega$, $R_2 = 30k\Omega$, $R_C = R_L = 2R_E = 4k\Omega$, $r_o = \infty$, $V_{BE} = 0.7$.



Considering low freq., capacitors' effect is not negligible. Hence, it'll limit gain now.
Low freq. model will differ now. Something like :-



Now, consider simplest model :-
(small signal → AC only)



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Note : Its AC signal.
So, if for +ve ½ cycle, i_b (i_c) is into base (collector) it'll be out of base (collector) for -ve ½ cycle. (making $i_e = i_b + i_c$, always)

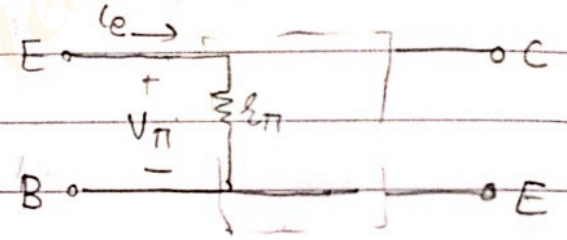
Now, finding r_π, g_m, r_e for simplistic model (before)

r_π → $\frac{v_{be}}{i_b}$

g_m → $\frac{i_c}{v_\pi} = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$

r_e → i.e. resistance as seen from emitter of CE Amp. OR, resistance of a proved before CB Amp :-

Also, $\beta = \frac{i_c}{i_b}$, $\alpha = \frac{i_c}{i_e}$

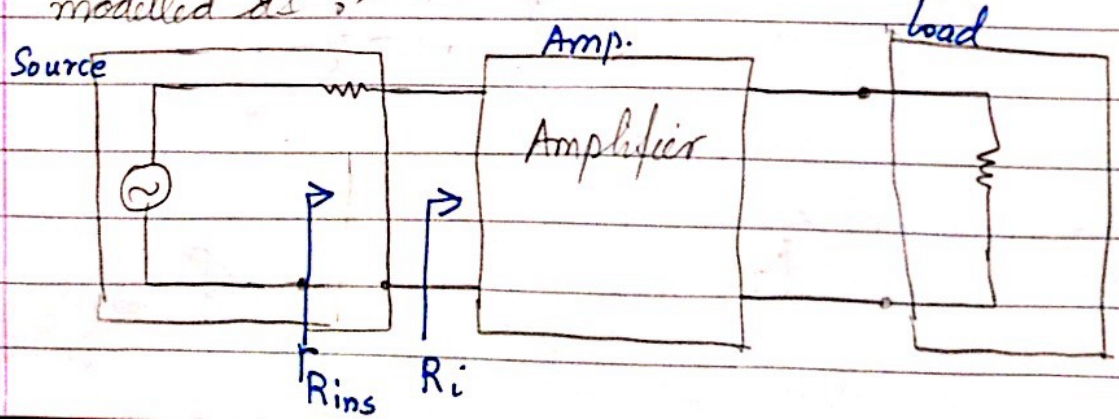


Using above eq^{ns}, we can prove that,

$r_\pi = \frac{V_T}{I_B}$, $r_e = \frac{V_T}{I_E}$

↳ So, we can get all values from DC bias cond^n. We can model after getting values.

Now, for given fig (eg.), amplifier sys can be modelled as :-



* Find o/p resistance : using test source method

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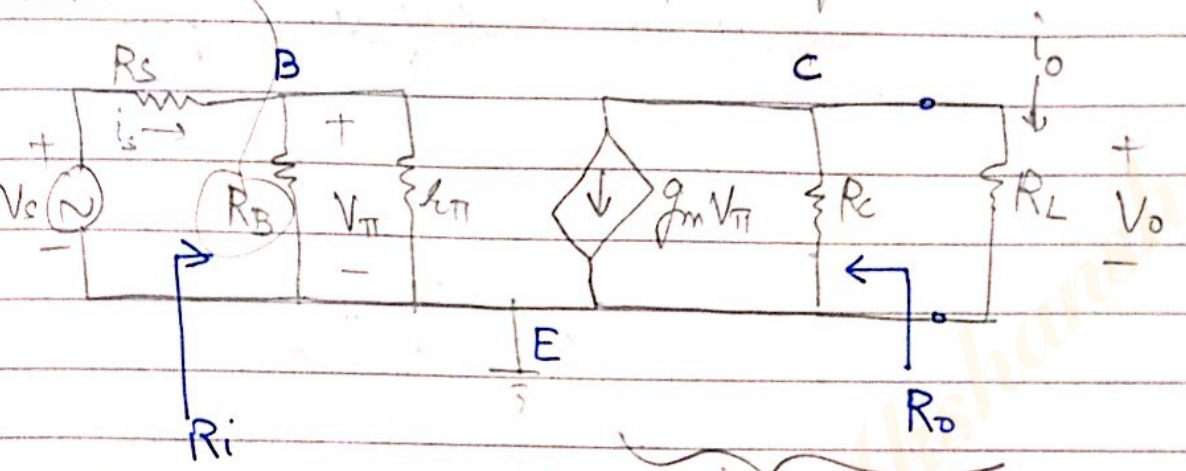
Now, removing all DC, solving, we get :-



$$V_o = (-g_m V_\pi)(R_C \| R_L)$$

$$R_i = R_B \| r_\pi$$

$$R_{ins} = R_S + (R_B \| r_\pi)$$

$$V_\pi = \frac{(R_B \| r_\pi)}{(R_B \| r_\pi) + R_S} \times V_s$$

Remove V_π, get g_m.

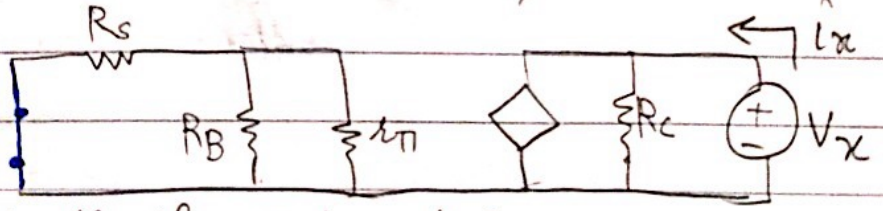
R_o

Test source method

S1) Identify o/p side

S2) Remove o/p resistance

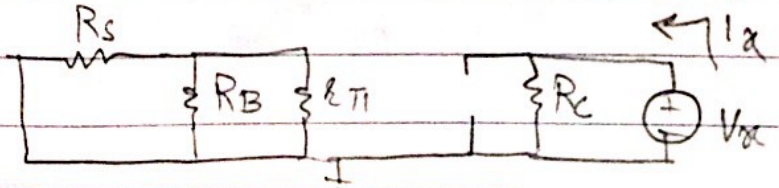
S3) Put a test source on its place (V_x, i_x)



S4) Short all other independent sources.

$\Rightarrow V_s = 0$ (SC) $\Rightarrow V_\pi = 0 \Rightarrow g_m V_\pi = 0$ ($\Rightarrow$ OC)

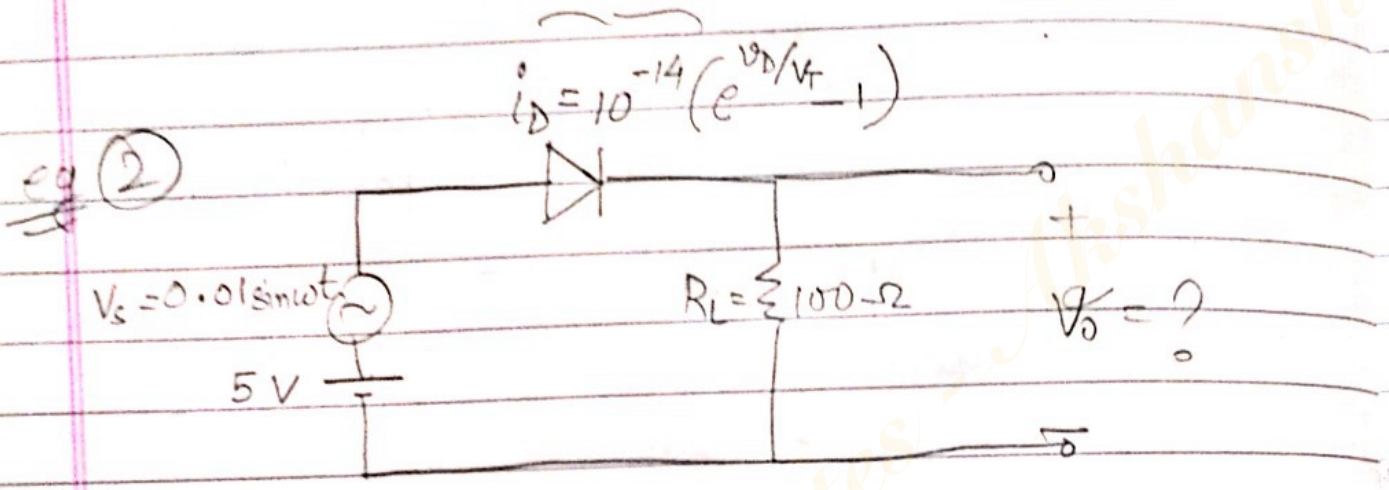
So, model is :



Now, in this model, $R_o = R_c = V_o / i_o$

had to been there (for ~~f~~ char.),

$R_o = R_c \| R_o$. (o/p resistance) ✓

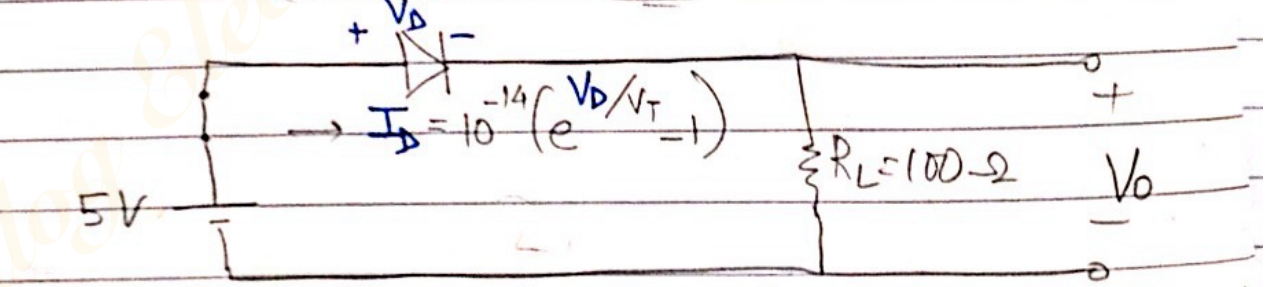


Find V_o = ? from above figure

↳ signal component of o/p voltage

S1) DC Analysis :

(a) Remove all AC



$-5 + V_D + V_o = 0$

$\Rightarrow V_o = 5 - V_D$.

$\Rightarrow R_L I_D + V_D = 5 \rightarrow (1)$

(b) Solve iteration to get V_D, I_D

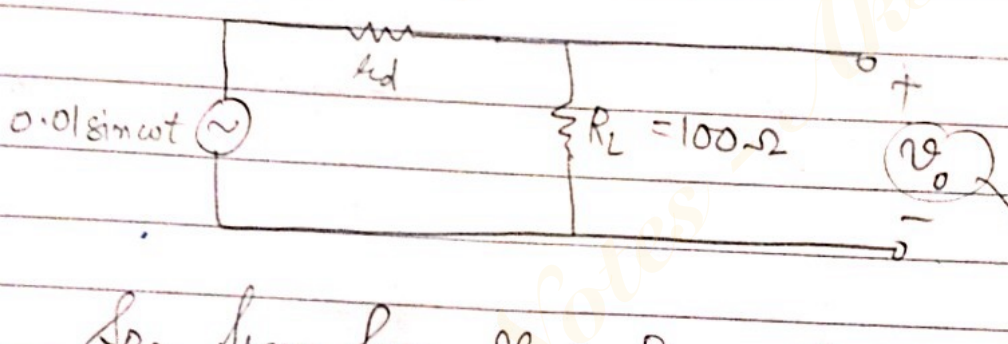
S2) Find AC diode resistance, r_d.

$$r_d = \frac{V_T}{I_D}$$ (proved before)

S3) Make AC model

↳ Replace diode by resistor

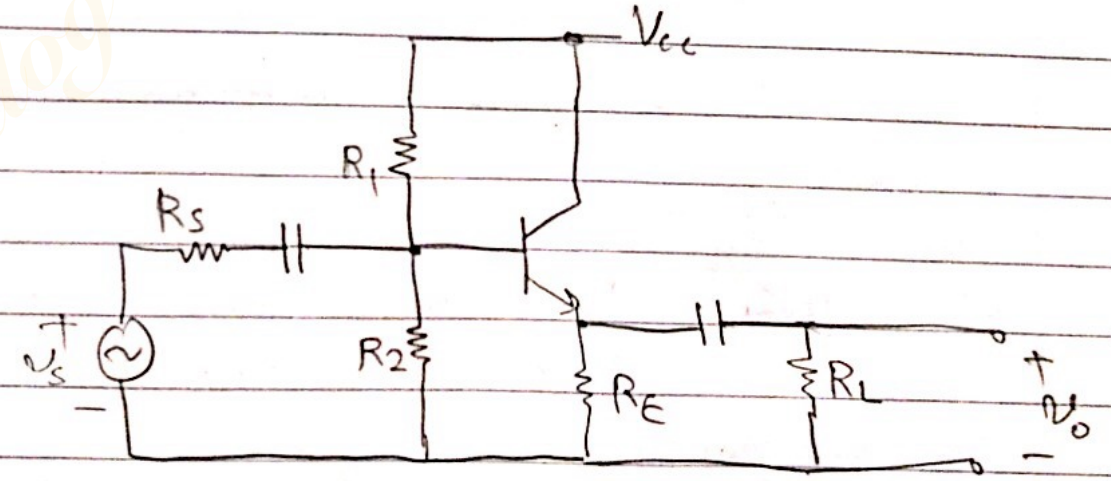
↳ Keep only AC components (kill DC)



So, from here, $v_o = \frac{R_L}{R_L + r_d} (0.01 \sin \omega t)$

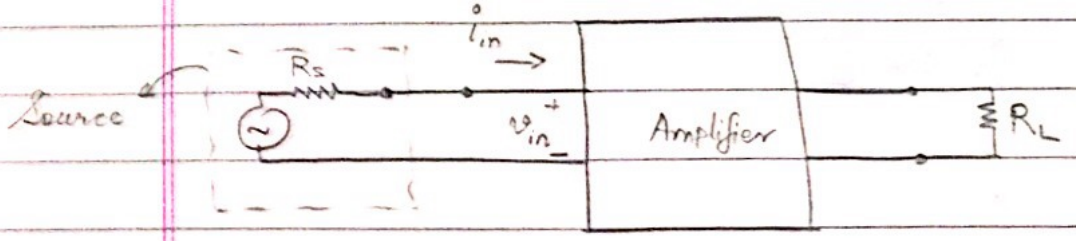
(voltage divider rule)

§ COMMON Collector Amplifier :-



It can similarly be modelled, & parameters can be found.

OPERATIONAL AMPLIFIERS AND CIRCUIT APPLICATIONS.

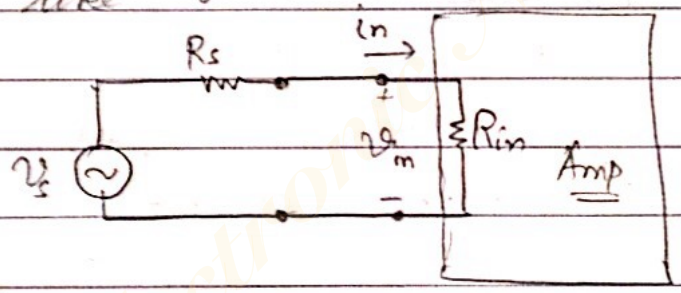


Idea: Amplifier connected to source should be s.t. it makes R_s immaterial

Considering i_{in} & v_{in} at i/p of Amplifier

So, $\exists \quad R_{in} = \dfrac{v_{in}}{i_{in}}$

So, i/p side looks something like:



✓ If $R_{in} = 1K\Omega$, $R_s = 100K\Omega$.

we have $v_{in} = \dfrac{R_{in}}{R_{in}+R_s} v_s \simeq 0.01 v_s$ (very small)

So, v_{in} doesn't depend much on v_s.

So, voltage across R_s is more, and just getting wasted.

✓ If $R_{in} = 100M\Omega$, $R_s = 100K\Omega$

$\Rightarrow v_{in} = \dfrac{100\times10^6}{100\times10^6 + 100\times10^3} v_s$

$\Rightarrow v_{in} \simeq v_s$. So, effect of R_s almost ignored.

$\hookrightarrow R_{in} \to \infty$

Puffin

"Emitter resistance should be zero ($\to 0$) so that $\exists$ no drop & load resistor fully effective

Ideal characteristics of an amplifier:

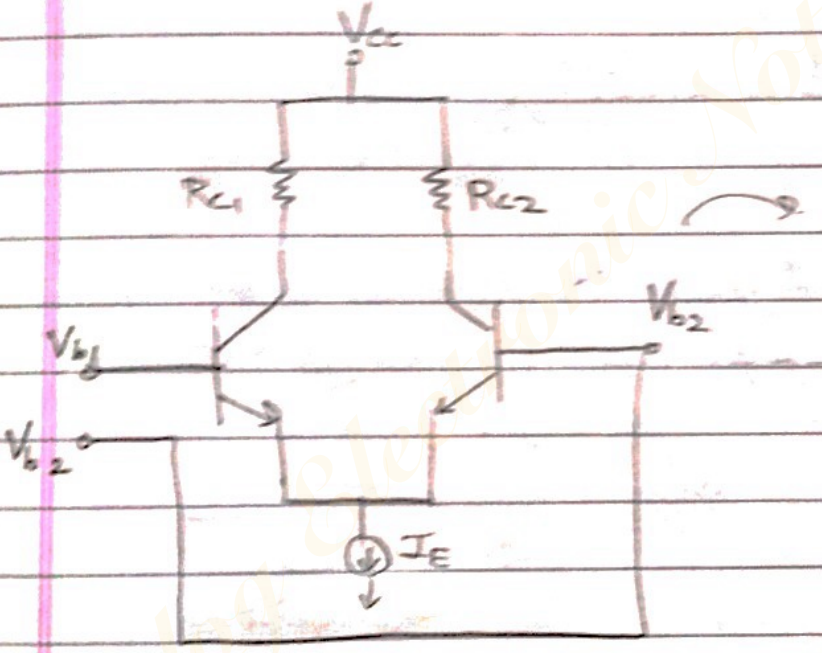
$R_{in} \to \infty$

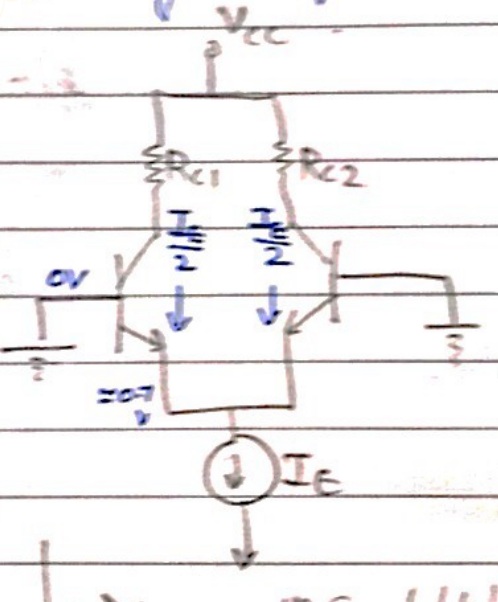
$R_o \to 0$

(A) $\to \infty$

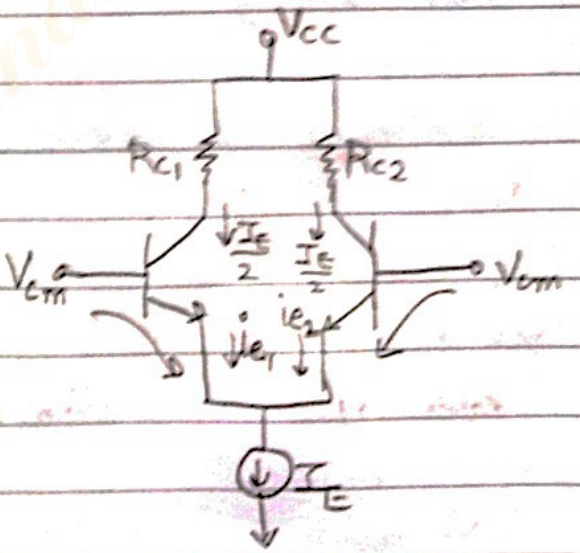
↳ gain $\to \infty$ b/c that it can amplify even a very small signal

- above cond^{n} are not met by single stage amps





↳ DC cond^{n} is established b/c, I_E, across R_{C1} & $R_{C2} = \frac{I_E}{2}$ each

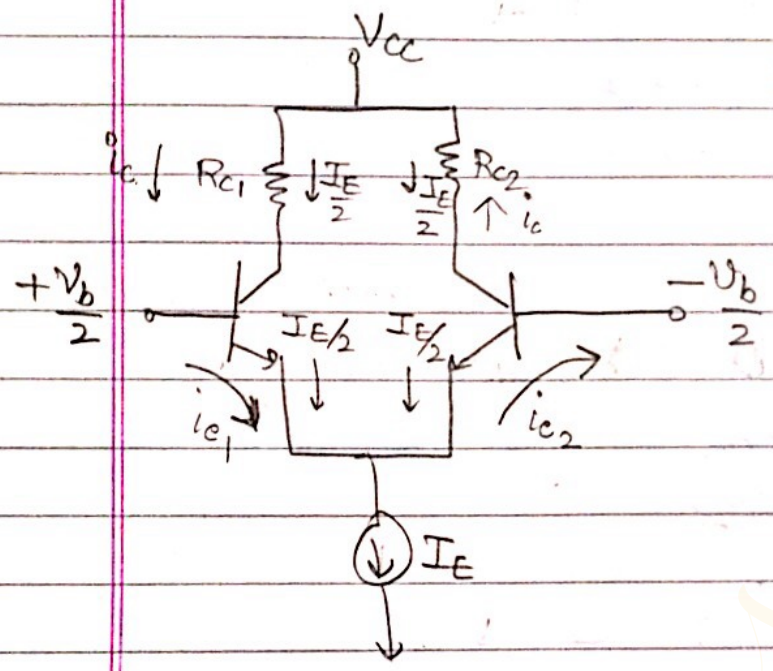


∴ If both bases are supplied by same voltage, $\exists$ extra current, i_{e1} & i_{e2} ($i_{e1} = i_{e2}$) along with $\frac{I_E}{2}$ on both sides.

b/c, current through $I_E = I_E + 2i_e$

Because current source at emitter is constant, so, it cannot take in → $\frac{I_E}{2} + \frac{I_E}{2} + i_{e_1} + i_{e_2}$.

So, $i_{e_1} = i_{e_2} = 0$ (no biasing happens)



$$I\big|_{R_{C1}} = \frac{I_E}{2} + i_c$$

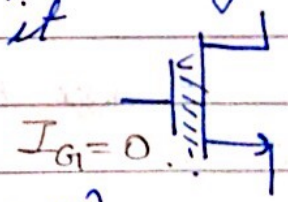
$$I\big|_{R_{C2}} = \frac{I_E}{2} - i_c$$

$$I\big|_{\text{current source at emitter}} = I_E + i_{e_1} - i_{e_2}$$

$$= I_E\big|_{i_{e_1} = i_{e_2}}$$

So, this model will work

* Replacing BJT with MOSFET is better because we can get high input impedance ($R_{in} \to \infty$)
  MOSFET: oxide layer prevents gate current flow across it

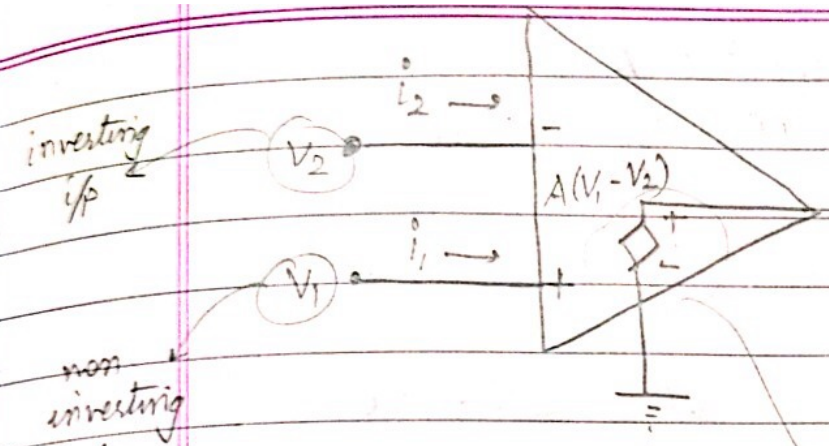


* For $A \to \infty$ (making gain $\to \infty$), put multiple stages of amplifiers.
* For $R_o \to 0$, certain o/p char. are changed.

The above model (with MOSFET) is represented ↗.

($V_1 = V_b/2$, $V_2 = -V_b/2$)

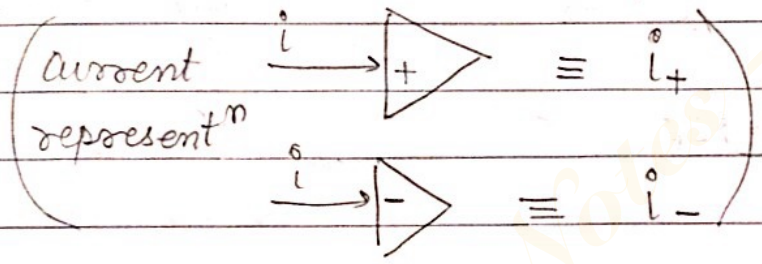
Ideal op-amp equivalent circuit.



→ represents controlled voltage source with value : $A(V_1 - V_2)$

* Ideally, $i_1 = i_2 = 0$ (to ensure $R_{in} \to \infty$)

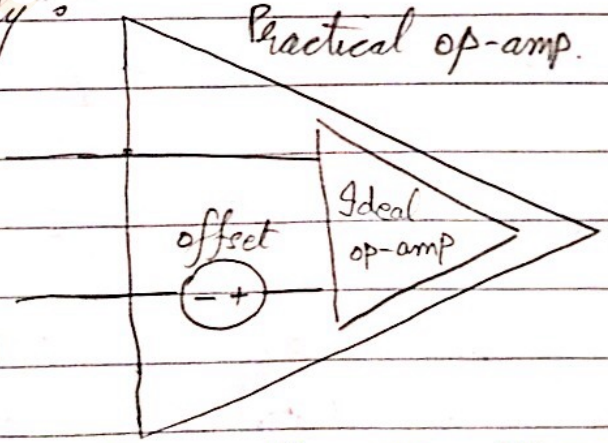
current representⁿ



• We placed 2 similar MOSFETS in differential pair configurⁿ. But, when placed like that, ∃ some offset.

So, some extra offset voltage is req to balance or make both FETs identical

So, basically:



Ideal op-amp : $A \to \infty$, $R_o = 0$, $R_{id} \to \infty$, $I_+ = I_- = 0$, $V_{offset} = 0$

$V_o = A(V_1 - V_2)$

We are supplying V_{cc} to op-amp.

So, under NO cond^n, $V_o > V_{cc}$ ↳ NEVER

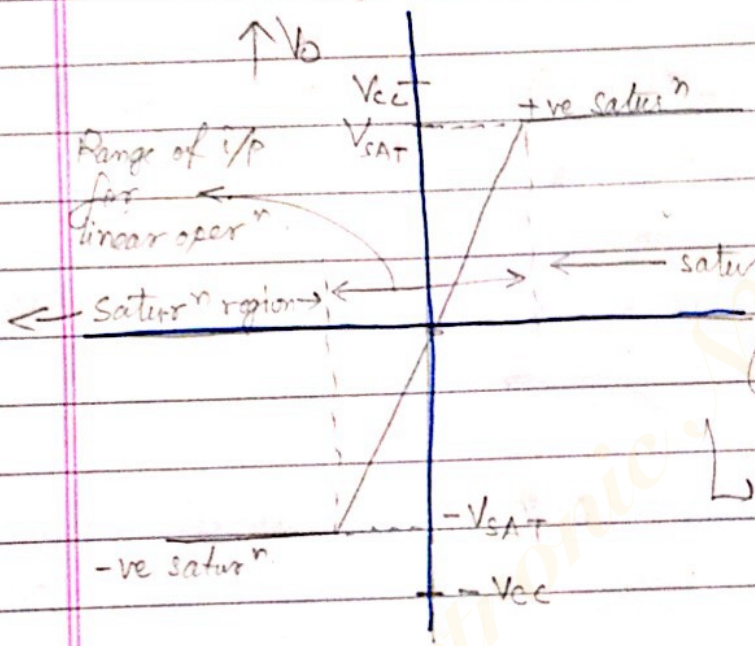
So, for $A \to \infty$

$V_o = A(V_1 - V_2)$

So, for V_o to be $< V_{cc}$,

$V_1 - V_2 \to 0$.

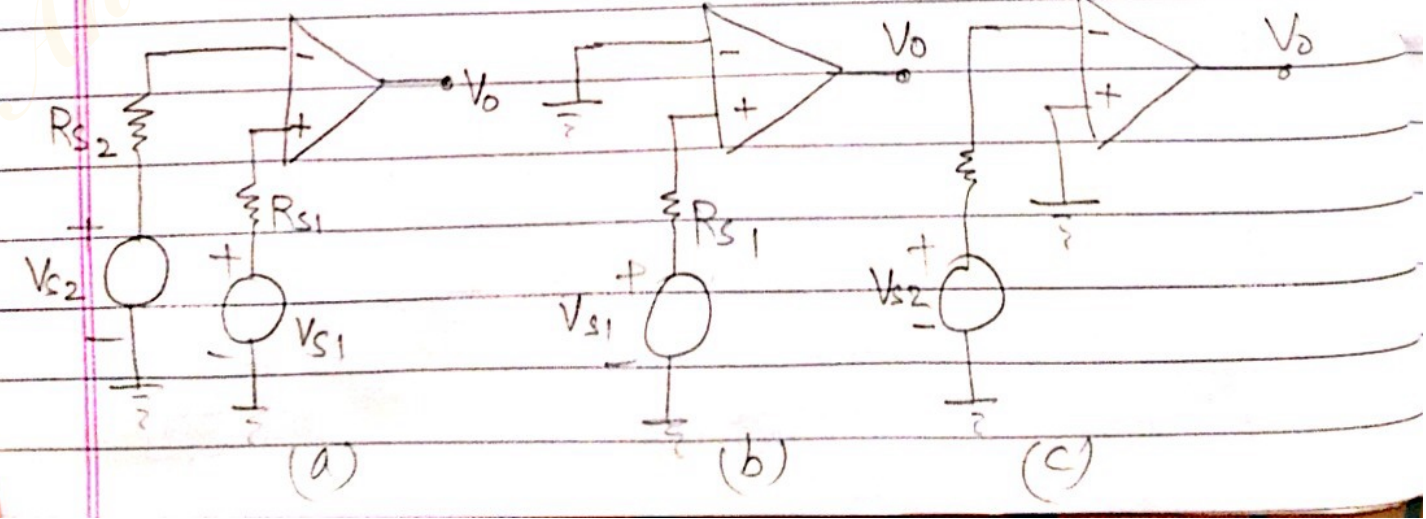
So, in most cases, we take $V_1 = V_2$ or $V_+ = V_-$



★ OP-AMP Transfer Characteristics

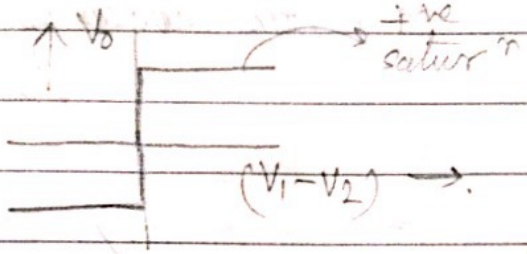
↳ Assumed :
A = finite (very large value)
(not infinite)

★ Open loop configur^n of Op-Amp.



Assuming $A \to \infty$

o/p transfer char :-



For (a), consider ideal op-amp, $\Rightarrow$ no current at i/p.

$\therefore V_+ = V_{S1}$ & $V_- = V_{S2}$

If $V_{S1} > V_{S2} \longrightarrow V_o = A(V_{S1} - V_{S2}) =$ +ve satur^n.

$V_{S1} < V_{S2} \longrightarrow V_o = A(V_{S1} - V_{S2}) =$ -ve satur^n.

for (b),

$V_{S2} = 0$,

V_{S1} = any value (+ve)

$V_o = A(V_{S1}) =$ +ve satur^n.

for (c)

$V_{S1} = 0$, V_{S2} = any value.

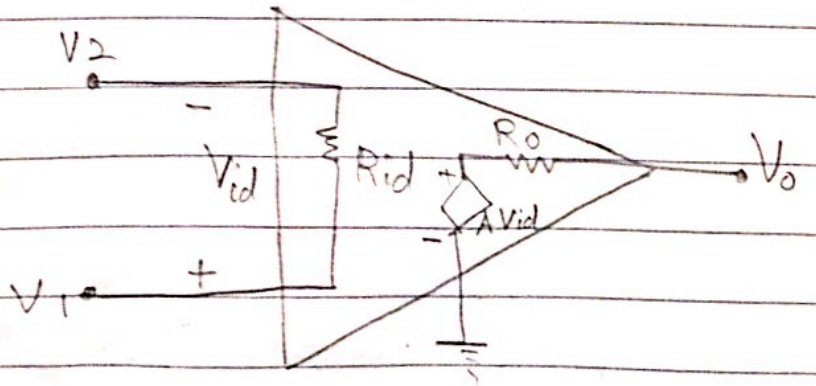
$\Rightarrow V_o = A(-V_{S2}) =$ -ve satur^n.

$\therefore$

in open-loop configur^n, op-amp behaves in +ve or -ve satur^n.

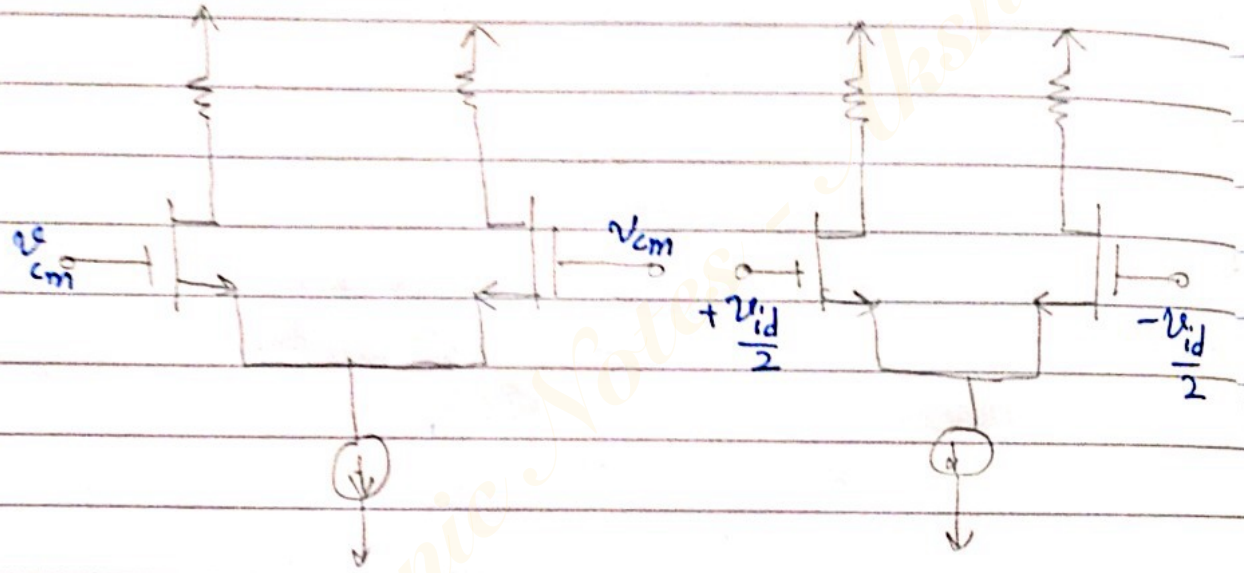
☆ NON IDEAL OP-AMP.

Equivalent circuit :-



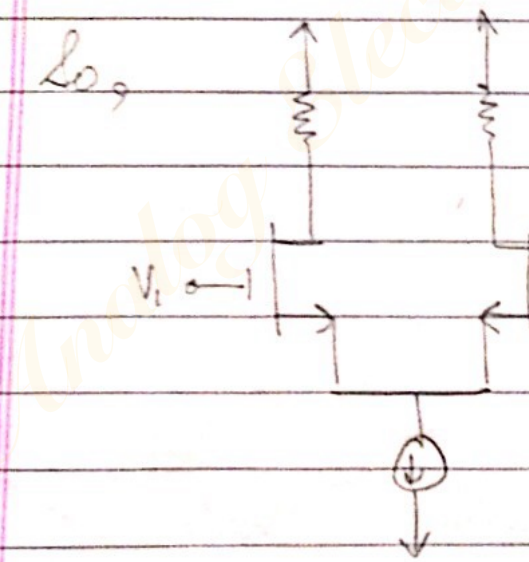
* When load is connected,
$V_o < AV_{id}$
(some drop across R_o)

* Op-Amp is said to have 2 types of i/p:
1. Common mode:
$$V_{cm} = (V_1 + V_2)/2$$
2. Differential mode:
$$V_{id} = V_1 - V_2$$



(Common mode) (Differential mode)

So,



We can write
$$V_1 = \frac{V_1+V_2}{2} + \frac{V_1-V_2}{2}$$
& $$V_2 = \frac{V_1+V_2}{2} - \frac{V_1-V_2}{2}$$

Idea:- let $\frac{V_1+V_2}{2} = x$

$$\frac{V_1-V_2}{2} = y$$

So, Case (1): Take both inputs = ^2x.
It is a common mode i/p.

Case ② :- Take inputs as y & $-y$.
Then, it's a differential mode i/p.

(Note :
$v_1 - v_2 = v_{id}$.
$\Rightarrow \pm\left(\frac{v_1 - v_2}{2}\right) = \pm\frac{v_{id}}{2}$.)

So, by Superpos^n principle,
Total o/p from amplifier = (o/p)$_{case①}$ + (o/p)$_{case②}$

So, $V_o = A_{cm} v_{cm} + A_d v_d$

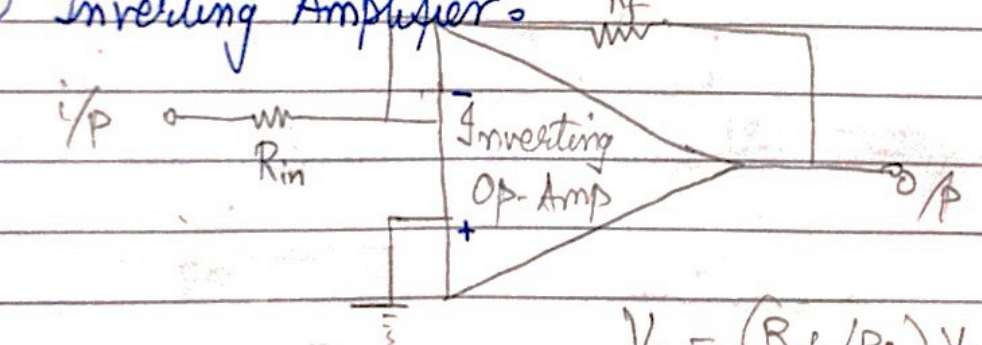
$A_{cm} v_{cm}$ → very small
$A_d v_d$ → very very large

$\rightarrow \frac{A_d}{A_{cm}}$ = CMRR (Common mode Rejection ratio)

$\frac{A_d}{A_{cm}} \rightarrow \infty$. (Ideally)

✱ OP-AMP with negative feedback :

① Inverting Amplifier :



$V_o = (R_f / R_{in}) V_s$

here, $V_+ = 0$ (GND).
for ideal case : $V_+ = V_- \Rightarrow V_- = 0$.

So, current through $R_1 = \frac{V_s - 0}{R_{in}}$

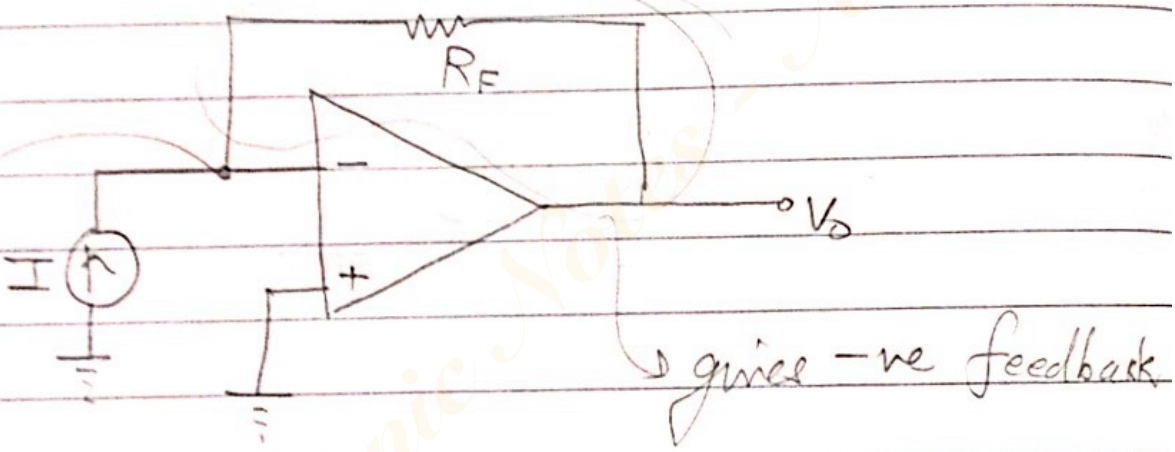
Now, ideal i/p amp $\Rightarrow i = 0$.

So, complete current goes through R_f

Now, current through $R_f = \frac{0 - V_o}{R_f}$

We have: $\frac{V_s - 0}{R_{in}} = \frac{0 - V_o}{R_f}$ *

Applic^{ns}: ① Current to voltage converter:

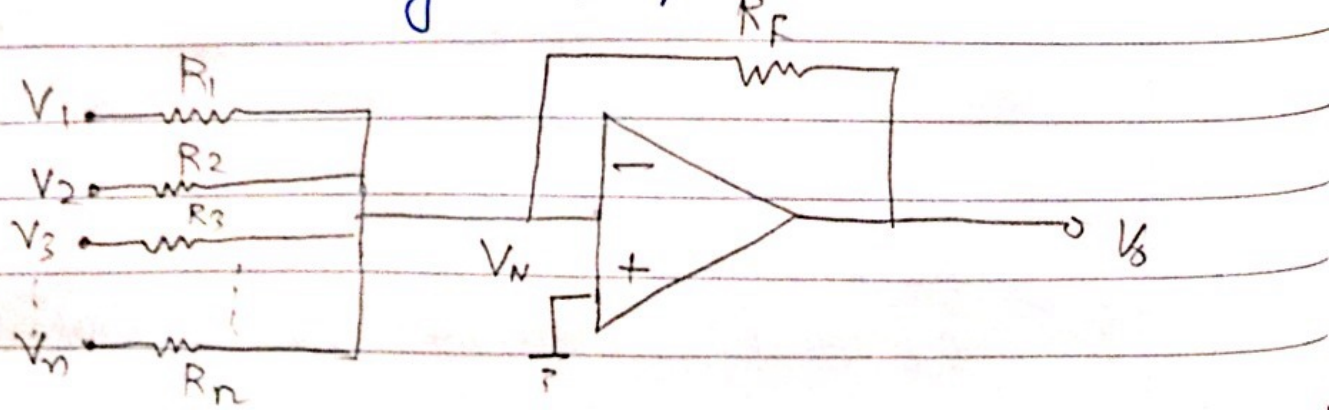


KCL: $I = \frac{0 - V_o}{R_F}$

$\Rightarrow V_o = -IR_F$

So, it's something like a current controlled voltage source.

② Summing amplifier:



Here, $V_+ = 0$. (Grounded)

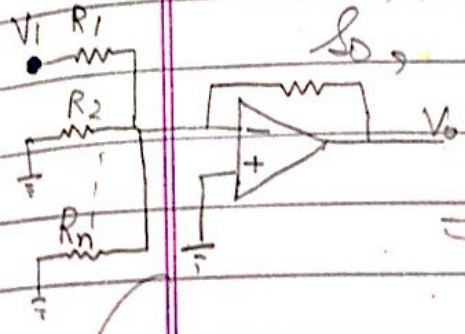
for ideal, $V_+ = V_-$.

$\Rightarrow V_- = 0$

Now, using o/p due to all i/p voltages.

Use : POS (principle of superposition)

So, take only V_1 (rest all voltages grounded),



So, $\frac{V_1 - 0}{R_1} = \frac{0 - (V_o)_{\text{due to 1st i/p}}}{R_f}$

$\Rightarrow V_{o1} = -R_F\left(\frac{V_1}{R_1}\right)$

$\Rightarrow V_o = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \dots + \frac{V_n}{R_n}\right)$

↳ If $R_1 = R_2 = \dots = R_n = R_F$

$\Rightarrow V_o = -(V_1 + V_2 + \dots + V_n)$

for ideal amp, $i_+ = i_- = 0$

↓

So, it like a summing amplifier. But, only thing is, it's inverting it (-ve sign ∃).

* Inverting op-amp : One (or many) i/p on inverting part (-ve)
* Non-inverting op-amp : One (or many) i/p on non-inverting part of op-amp (+ve)

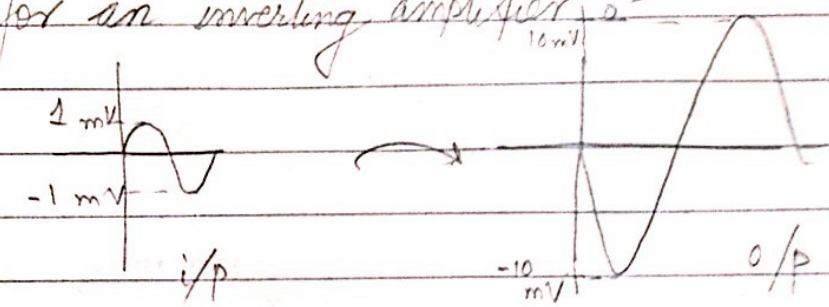
* Property of op-amp : It can accept any type of signal.

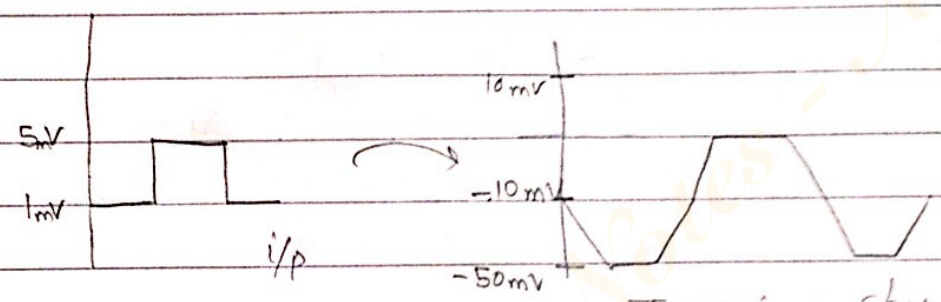
↳ given a sq. wave i/p → SLEW RATE comes into picture.

EFFECTS OF SLEW RATE

For a sq. wave i/p, amplifier won't be able to rise & fall at the same rate. So, response of op-amp becomes sluggish

* for an inverting amplifier :-

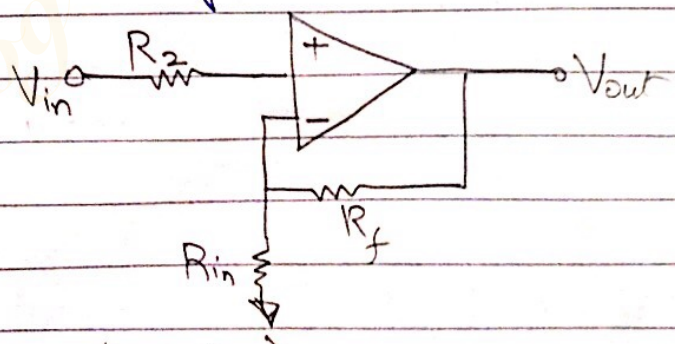




Trapezium shape

↓ becomes triangular when freq. of i/p becomes high

(B) Non-Inverting Amplifier :-



$$V_{out} = \left(1 + \frac{R_f}{R_{in}}\right) V_{in}$$

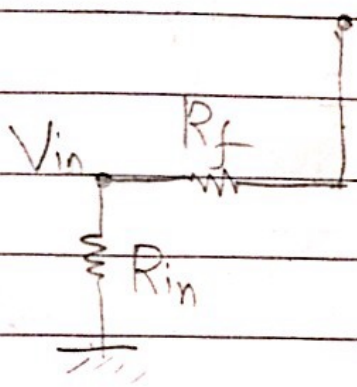
For ideal amp, $i_+ = 0$

$\Rightarrow R_2 = 0$ (SC)

$\Rightarrow V_+ = V_{in}$

Also, $V_+ = V_- \Rightarrow V_- = V_{in}$

So, we have :-



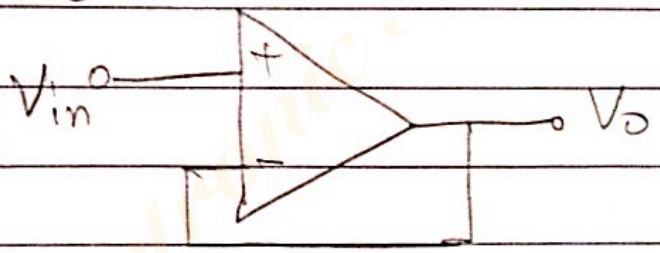
$\Rightarrow \frac{V_{in}}{R_{in}} = \frac{V_o}{R_f + R_{in}}$

$\Rightarrow V_{in} = \left(\frac{R_{in}}{R_f + R_{in}}\right) V_o$.

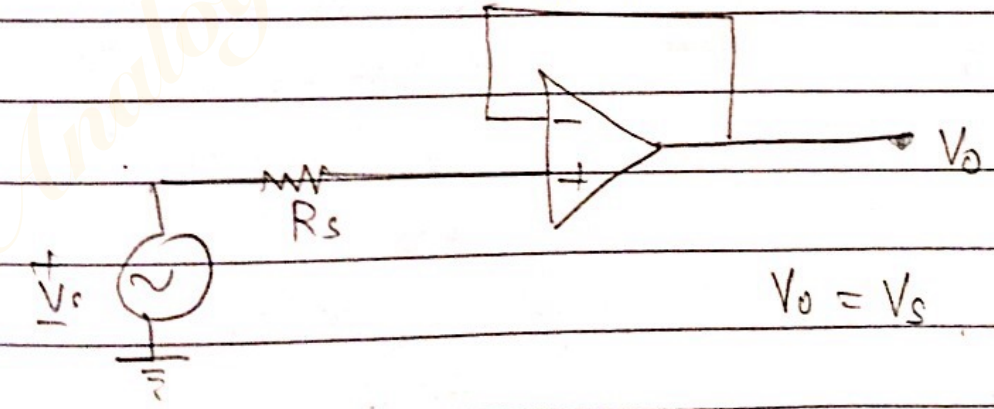
↳ for $V_o = V_{in}$,

$R_f \to 0$ & $R_{in} \to \infty$.

So, we have :-



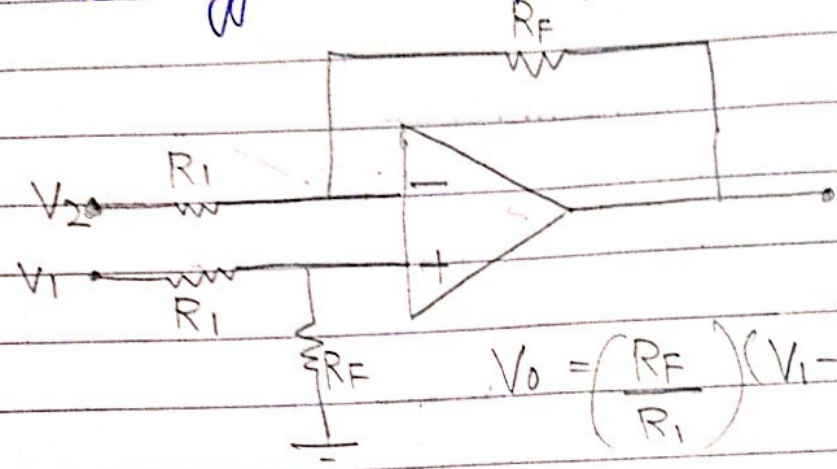
Applications : (1) Voltage follower :



$V_o = V_s$

o/p amplifies i/p's difference

(2) Difference Amplifier



$$V_0 = \left(\frac{R_F}{R_1}\right)(V_1 - V_2)$$

Seeing its working ; POS ;

Consider V_1 only ⇒ V_2 - GND , o/p voltage = V_{01}

It behaves as non inverting amplifier

Now, $V_{01} = \left(1 + \frac{R_F}{R_1}\right) V_+$

$$= \left(1 + \frac{R_F}{R_1}\right)\left[\frac{R_F}{R_F + R_1}\right] \times V_1$$

(V_+)

$$\Rightarrow V_{01} = \left(\frac{R_F}{R_1}\right) V_1$$

Consider V_2 ⇒ V_1 = GND (↳ $V_+ = 0$) , o/p voltage = V_{02}

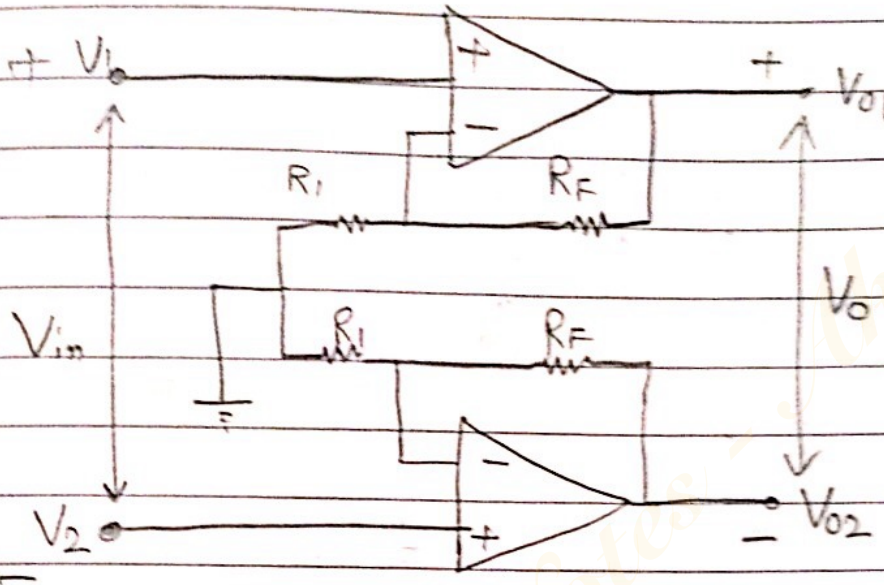
$$V_{02} = -\left(\frac{R_F}{R_1}\right) V_2$$

Overall voltage = $V_{01} + V_{02}$

$$= \frac{R_F}{R_1}(V_1 - V_2)$$

So, that's how a difference amplifier works. (Amplifⁿ done by adjusting R_F & R_1)

✱ Differential i/p differential o/p Amplifier :



$V_{O1} = \left(1 + \frac{R_F}{R_1}\right) V_1$

$V_{O2} = \left(1 + \frac{R_F}{R_1}\right) V_2$

$\therefore V_O = V_{O1} - V_{O2}$

$= \left(1 + \frac{R_F}{R_1}\right)(V_1 - V_2)$

$\therefore V_O = \left(1 + \frac{R_F}{R_1}\right) V_{in}$

V_{in} = differential i/p ≡ diff b/w V_1 & V_2

$$V_O = \left(1 + \frac{R_F}{R_1}\right) V_{in}$$

→ $V_1 - V_2$

→ $V_{O1} - V_{O2}$

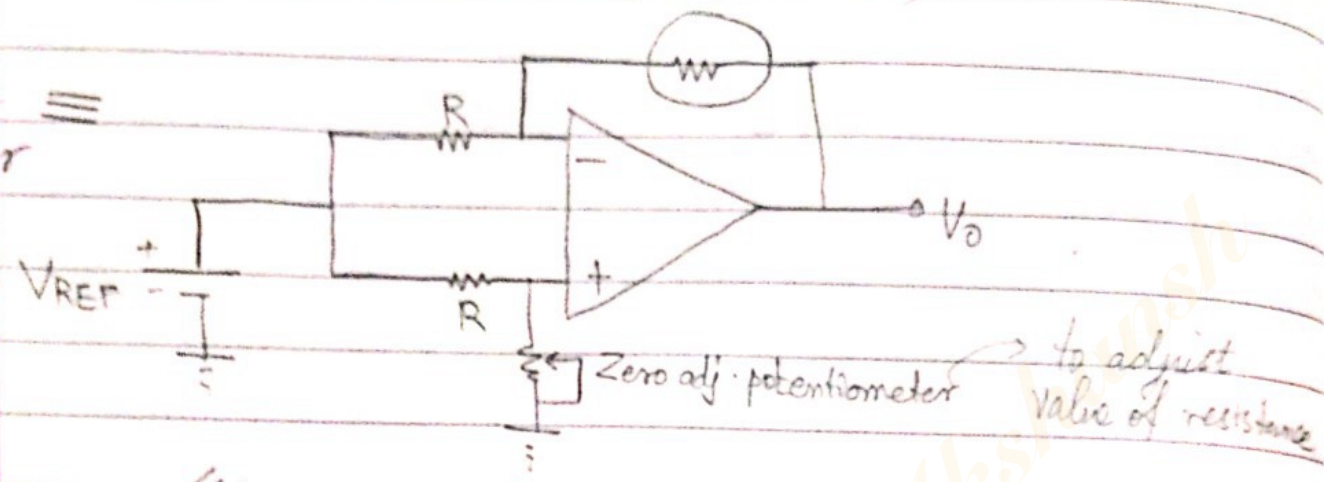
Recap : ✱ op-amp : at its i/p terminal → $R_{in} \to \infty$

o/p terminal → $R_O \to 0$.

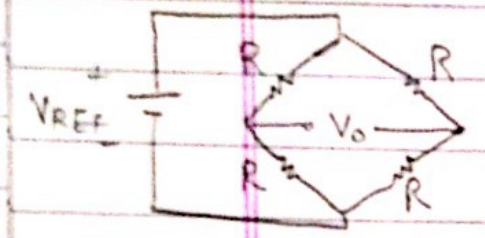
- can operate for DC & AC i/p.
- has low offset
- has very high gain (ideally $A \to \infty$)

↳ Hence, it can accomplish various operations.

(3) Bridge Amplifier



$$V_o = (-/+ V_{REF}) \cdot (\Delta R / 2R)$$

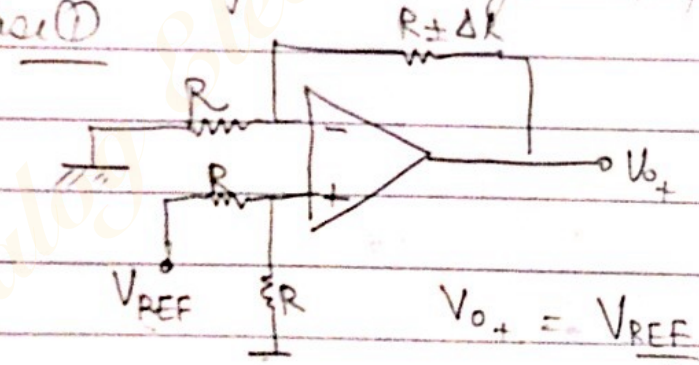


* 4 arms of wheatstone bridge can be made in bridge amplifier, as shown. Now, for ← circuit, we can have very small value of V_o. This value can be amplified by Bridge amplifier.

This makes this amplifier very sensitive.

Now, seeing the bridge amplifier by POS:

Case (1)

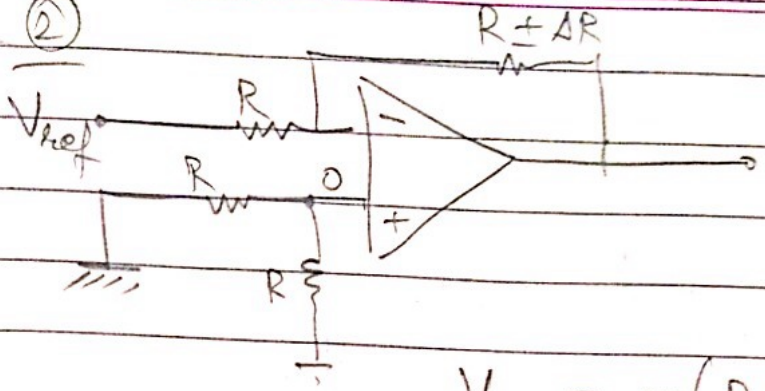


$$V_{o+} = \frac{V_{REF}}{2}\left[1 + \frac{R \pm \Delta R}{R}\right]$$

$$\Rightarrow V_{o+} = \frac{V_{ref}}{2}\left[2 \pm \frac{\Delta R}{R}\right] \rightarrow (1)$$

Note * The bridge amplifier behaves as a Temp. sensor

Case (2)



≡ Inverting Amp.

$$V_{o-} = -\left(\frac{R \pm \Delta R}{R}\right) \cdot V_{ref}$$

$$\Rightarrow V_{o-} = -\left(1 \pm \frac{\Delta R}{R}\right) V_{ref} \rightarrow (2)$$

Overall, $V_o = V_{o+} + V_{o-}$

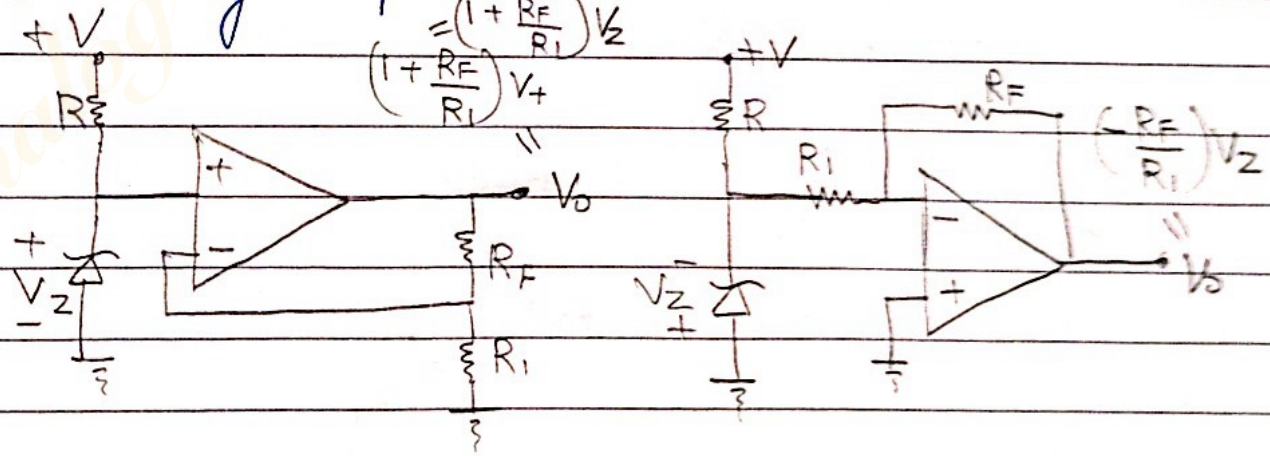
$$= \pm \frac{V_{ref}}{2}\left(\frac{\Delta R}{R}\right) \mp V_{ref}\left(\frac{\Delta R}{R}\right)$$

let $V_{Ref}\left(\frac{\Delta R}{R}\right) = \alpha$

$$= \pm \frac{\alpha}{2} \mp \alpha$$

$$= \mp \frac{\alpha}{2} = \mp \frac{V_{Ref}}{2}\left(\frac{\Delta R}{R}\right)$$

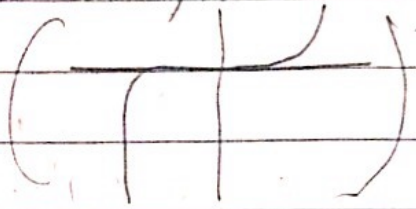
(4) Voltage References



Non inverting Voltage reference. (+ive voltage reference)

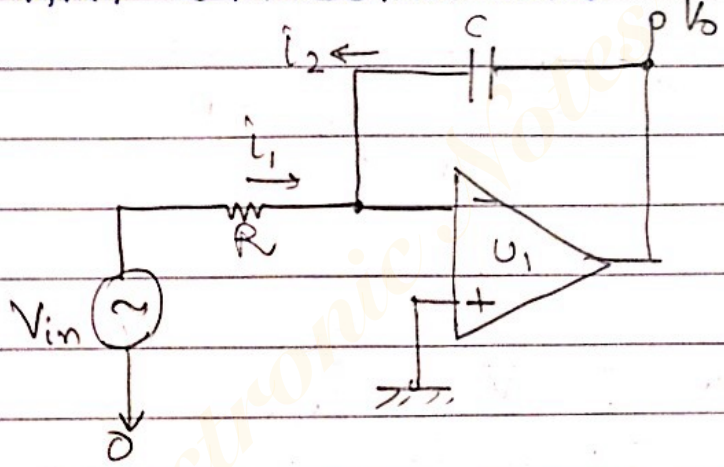
Inverting voltage reference (−ve voltage reference)

Idea: This is used when we want to supply const voltage.
Zener diode can operate at const voltage in RB.



So, we use Zener diode in RB mode.
(Vz stays constant)

✡ OP-AMP INTEGRATOR



Here, we are using a capacitor in circuit.
We know, capacitor blocks DC. So, use AC source

Now, $V_+ = GND$

$\Rightarrow$ for ideal, $V_- = 0$.

So,

$$i_1 = \frac{V_{in} - 0}{R} \rightarrow (1)$$

By KCL, $i_1 = -i_2 \rightarrow (2)$

Also,

$$i_2 = C \frac{d(V_o - 0)}{dt} \rightarrow (3)$$

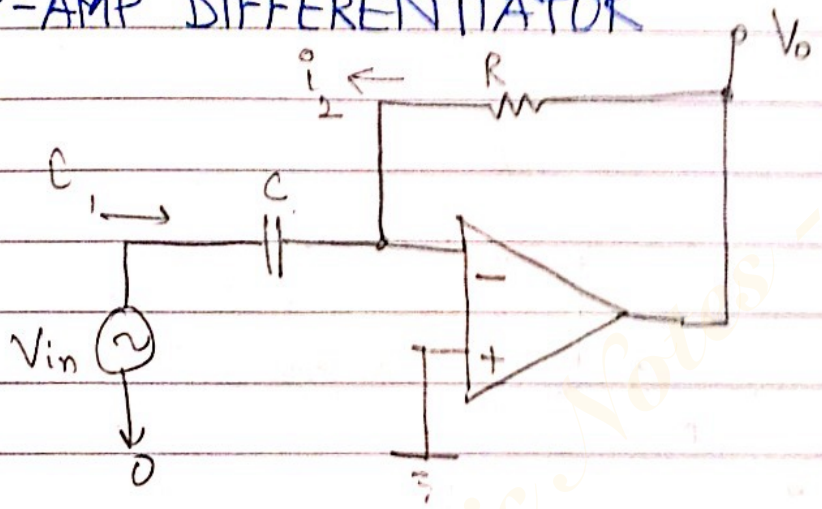
$\Rightarrow \frac{V_{in}}{R} = -C\frac{dV_o}{dt}$ (from ①, ② & ③)

$\Rightarrow V_o = \int(\,)V_{in}$

$\Rightarrow$ Circuit acts like an integrator

If $V_{in} = DC$ ($\equiv$ ramp), $\int(\,)V_{in} \neq 0$

✱ OP-AMP DIFFERENTIATOR



$V_+ = 0 \Rightarrow V_- = 0$

$\Rightarrow i_1 = C\left(\frac{d(V_{in}-0)}{dt}\right)$ → ①

& $i_1 = -i_2$

& $\frac{V_o - 0}{R} = i_2$

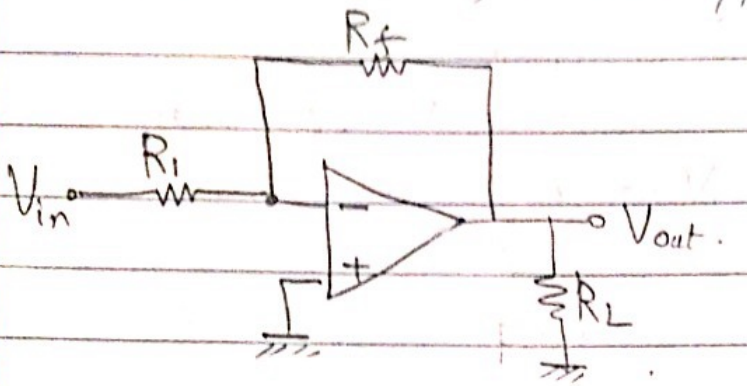
$\Rightarrow C\frac{dV_{in}}{dt} = -\frac{V_o}{R}$

$\Rightarrow V_o = (\,)\frac{d}{dt}V_{in}$

→ behaves as differentiator.

✱ Note :- op-amps can take input with $R_{in} \to \infty$ & give o/p with $R_o \to 0$. So, they can be used before any circuit.

Q Given the circuit, show, o/p resistance, $R_o = 0$



Test. source method

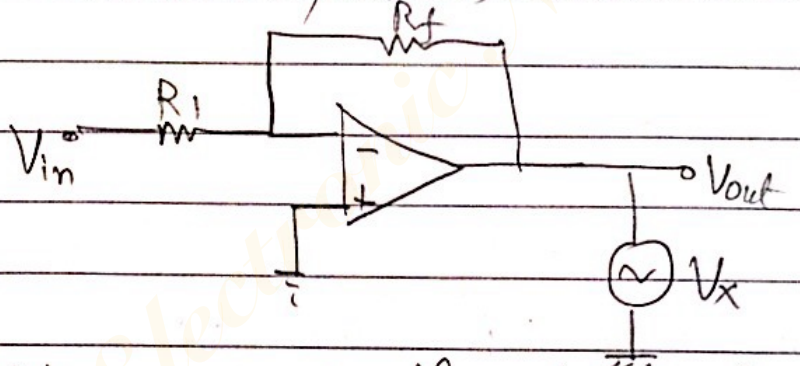
• General procedure to find o/p resistance of any circuit

Idea: We want to find R when looking from o/p side.

In general, an op-amp will drive some load, say R_L.

S1) Find where load is connected. Remove it

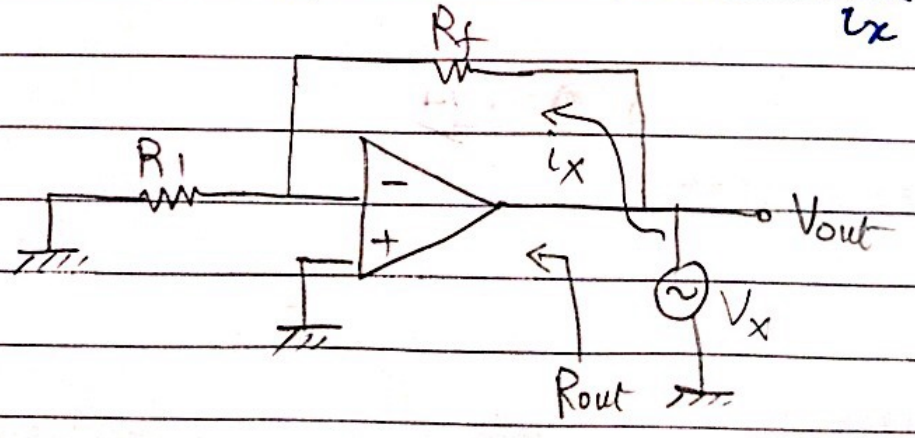
S2) Instead of load, connect a test source, V_x



S3) Now, we want effect of V_x. So, kill all other sources (Ground them)

If V_x supplies current i_x,

o/p resistance, $R_{out} = \frac{V_x}{i_x}$



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S4) Since $i/p = 0$ (Grounded), current sent by op-amp $= 0$. current (i_x)

Now, test source, that has been applied goes across R_f. Now, it cannot move further ∴ no potential difference

$$\Downarrow$$

$$i_x = 0.$$

$$\Rightarrow V_x = i_x (R_f + R_i)$$

$$= 0.$$

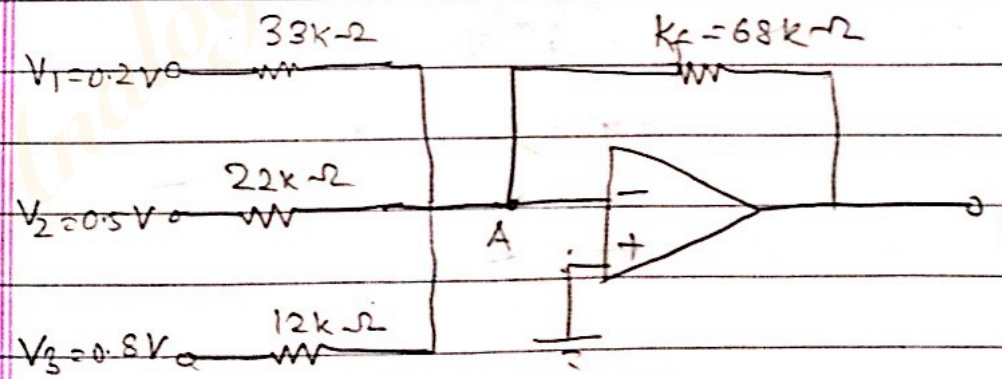
i.e, as soon as an external source was connected, it was pulled to zero.

$$\Downarrow$$

A short circuit is present over the region

$\Rightarrow$ output resistance $= 0$.

Q. Find V_o of the op-amp circuit :-



It is an inverting adder

★ From circuit, if an ideal op-amp has a -ve feedback, then $V_+ = V_-$

Here, $V_+ = 0$

$\Rightarrow V_- = 0 \Rightarrow V_A = 0$.

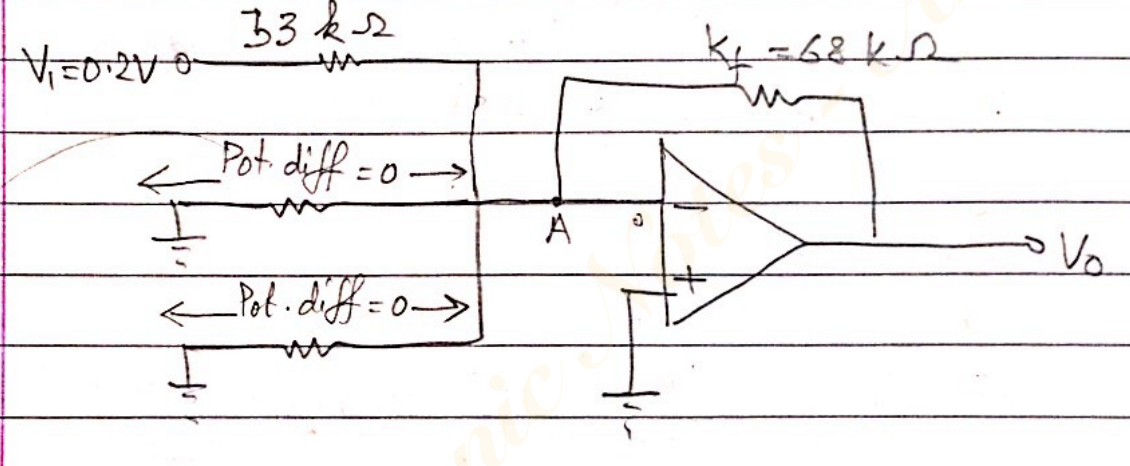
Now, principle of superposition (POS)

V_1, V_2, V_3 are 3 simultaneous i/ps

So, analysing each separately using POS

Case ①: Taking V_1 only

$\Rightarrow$



$\Rightarrow$ no current flows.

Now, current through $33k\Omega = \frac{0.2 - 0}{33k}$

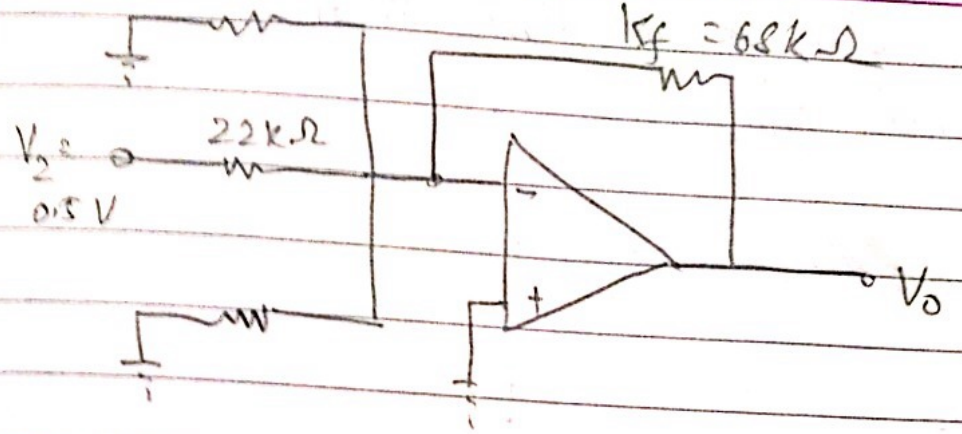
Also, by KCL, $i\big|_{\text{through } 33k\Omega} = i\big|_{\text{through } 68k\Omega}$

$\Rightarrow \frac{0.2 - 0}{33k} = \frac{0 - V_{01}}{68k}$

$\Rightarrow \frac{68k}{33k}(-0.2) = (V_0)_{\text{due to 1}}$

$\Rightarrow (V_0)_1 = -\frac{0.2}{33} \times 68$

Case ②: Taking V_2 only



On similar lines,

$$V_{o2} = -\left(\frac{0.5}{22}\right) \times 68$$

Case (3) :-

& $$V_{o3} = -\frac{0.8}{12} \times 68$$

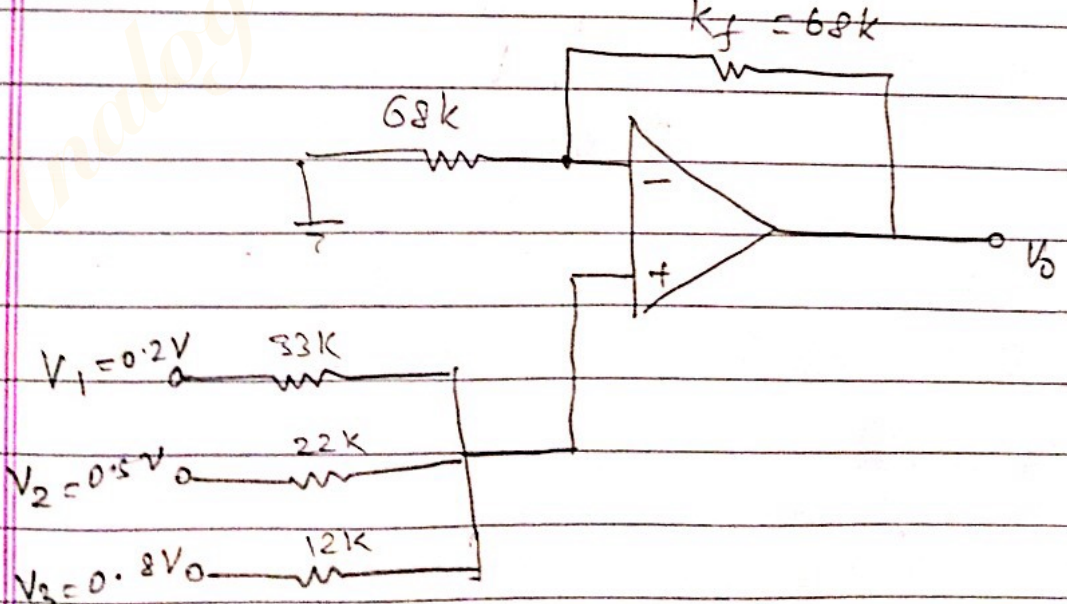
So, overall

$$V_o = V_{o1} + V_{o2} + V_{o3}$$

$$\Rightarrow V_o = -\left(\frac{0.2}{33} + \frac{0.5}{22} + \frac{0.8}{12}\right) \times 68 \quad \text{Volt}$$

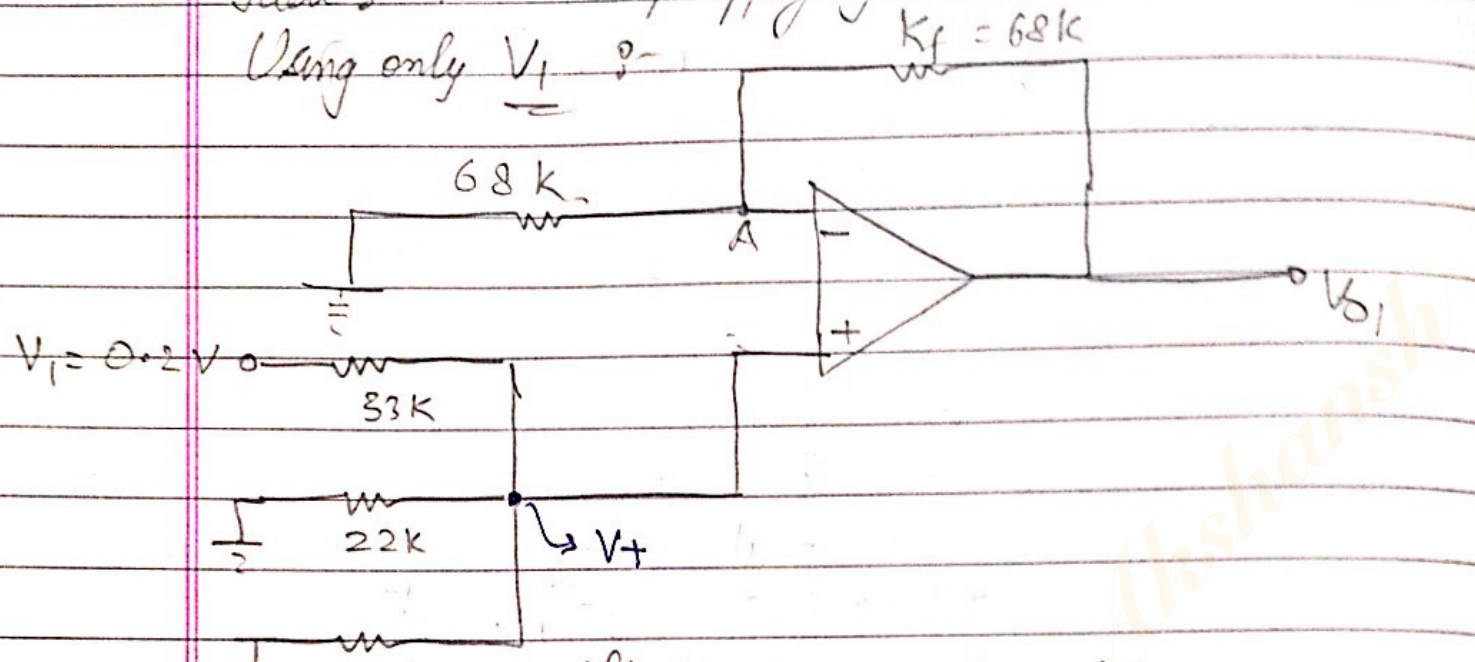
Ans

Extra : what if the i/p's are non-inverting?



Idea: Still keep applying POS.

Using only V_1 :-



This is a non inverting op-amp.

So, $o/p = \left(1 + \frac{R_f}{R_i}\right) V_+$

$= \left(1 + \frac{68k}{68k}\right) (V_+)_1$

Now,

$(V_+)_1 = \frac{22 \| 12}{33 + 22 \| 12} \times 0.2$ (Voltage divider)

$\Rightarrow V_{o1} = \left(1 + \frac{68}{68}\right) (V_+)_1$

$= 2 (V_+)_1$

Case ② :- Only V_2

$V_{o2} = 2 (V_+)_2 = 2 \left(\frac{33 \| 12}{33 \| 12 + 22} \times 0.5 \right)$

& $V_{O3} = 2(V_+)_3 = 2\left[\frac{33\|22}{33\|22+12} \times 0.8\right]$.

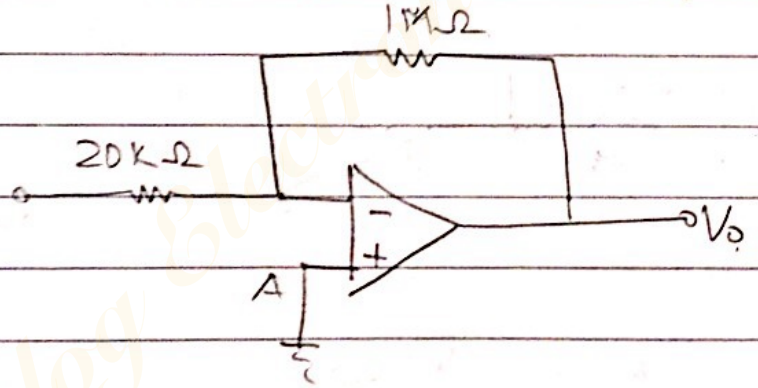
So, totally,

$$V_o = V_{O1} + V_{O2} + V_{O3}$$
$$= 2(V_+)_1 + 2(V_+)_2 + 2(V_+)_3.$$

$$\Rightarrow V_o = 2\left[\frac{22\|12}{33+22\|12} \times 0.2\right] + 2\left[\frac{33\|12}{33\|12+22} \times 0.5\right] + 2\left[\frac{33\|22}{33\|22+12} \times 0.8\right]$$

Ans

Q: What i/p voltage results in an o/p of 2V in the circuit shown?—



Here, Gain $= -\frac{1M\Omega}{20K\Omega} = -50$.

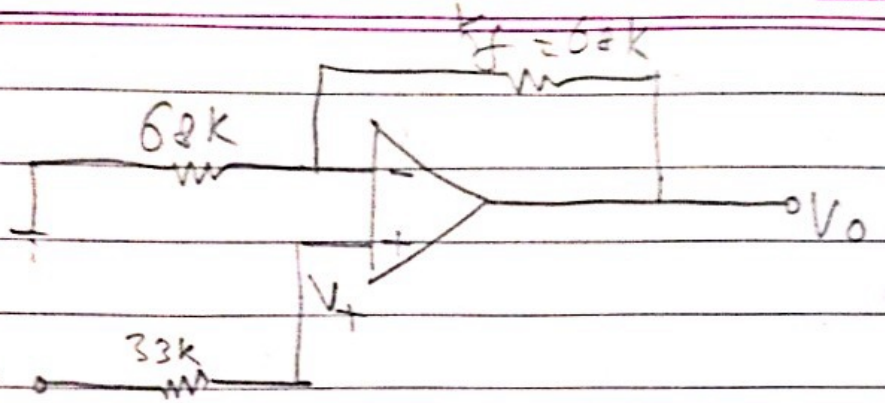
$$\Rightarrow \frac{V_o}{V_i} = -50$$

For $V_o = 2$, given

$$\Rightarrow V_i = -\frac{2}{50} = -\frac{1}{25} = -0.04\ V.$$

Ans

Note :

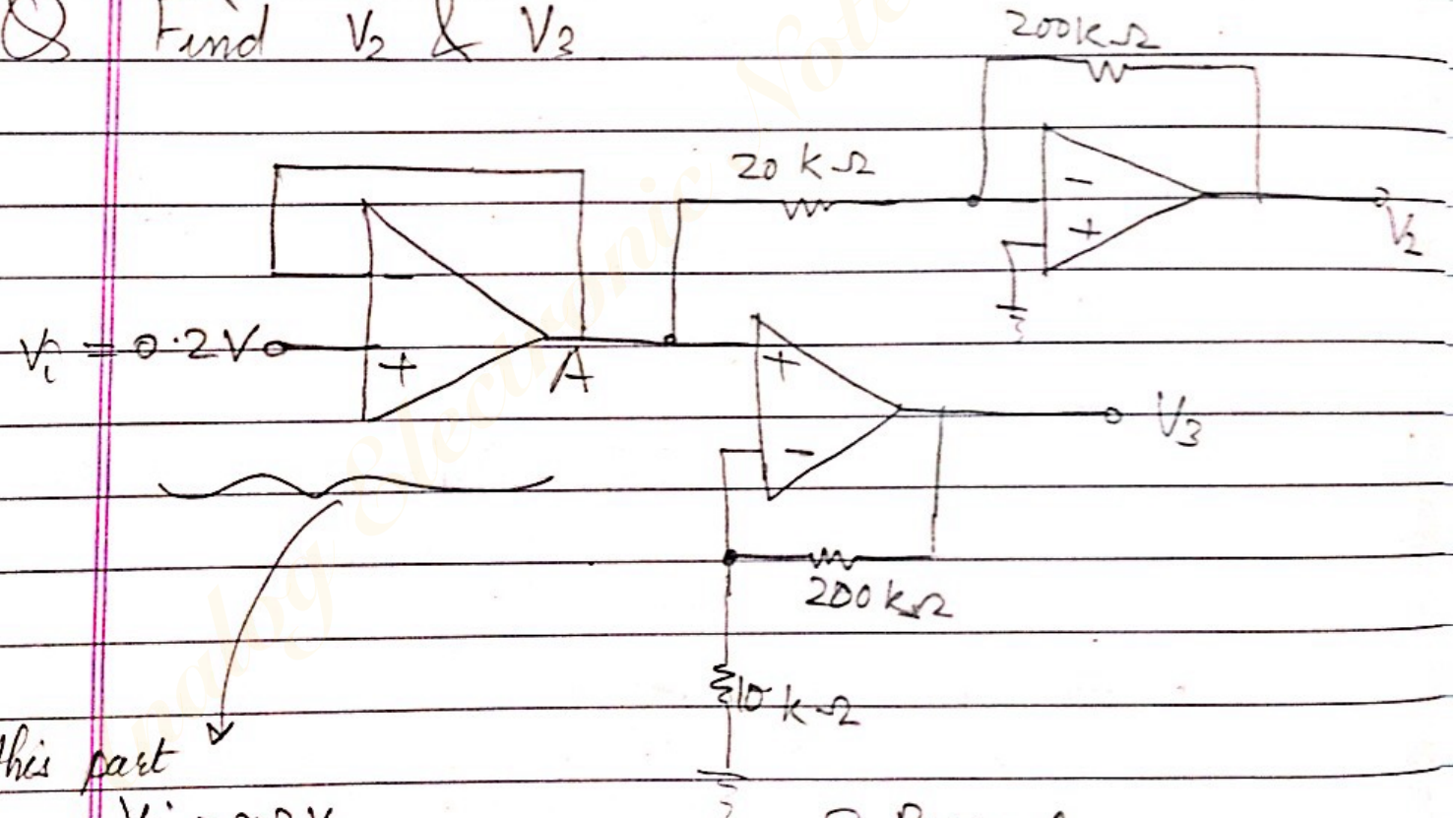


If we have such a configuration, note that potential diff across 33 kΩ = 0

So, no current flows across 33 kΩ

$\Rightarrow V_+ = V_1 = 0.2$ V.

Q Find V_2 & V_3



In this part

$V_i = 0.2$ V.

Also, $V_+ = V_- = 0.2$

So, $V_A = 0.2$ V

$\Rightarrow$ o/p = i/p.

So, why use this part ?

Reason :

It is a unity gain buffer

We want o/p to have a very small o/p resistance, which can only be given by op amp

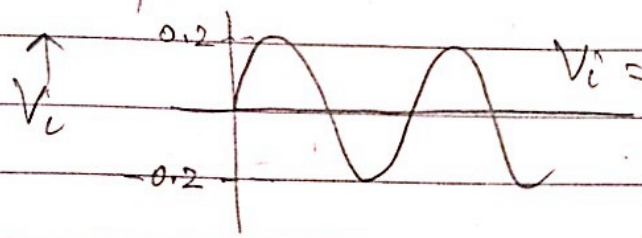
So, high i/p Resistance → low o/p resistance

Inverting op-amp.

$$V_2 = -\left(\frac{200}{20}\right) \times 0.2 = -2\ V.$$

$$V_3 = \left(1 + \frac{200}{10}\right) 0.2 = 4.2\ V$$

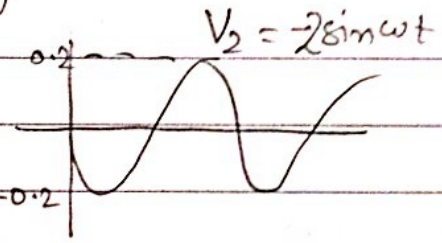
Extra: Suppose V_i = AC source now.



Now, finding V_2 & V_3.

Previously, $V_2 = -2\ V$. So, amplitude = 2 V, but it was inverted in phase by 180°.

So, V_2 becomes $-2 \sin \omega t$



& $V_3 = 4.2\ V$. So, it becomes $4.2 \sin \omega t$.

Note:- From trigonometry:-

$$\sin 3\omega t = 3 \sin \omega t - 4 \sin^3 \omega t.$$

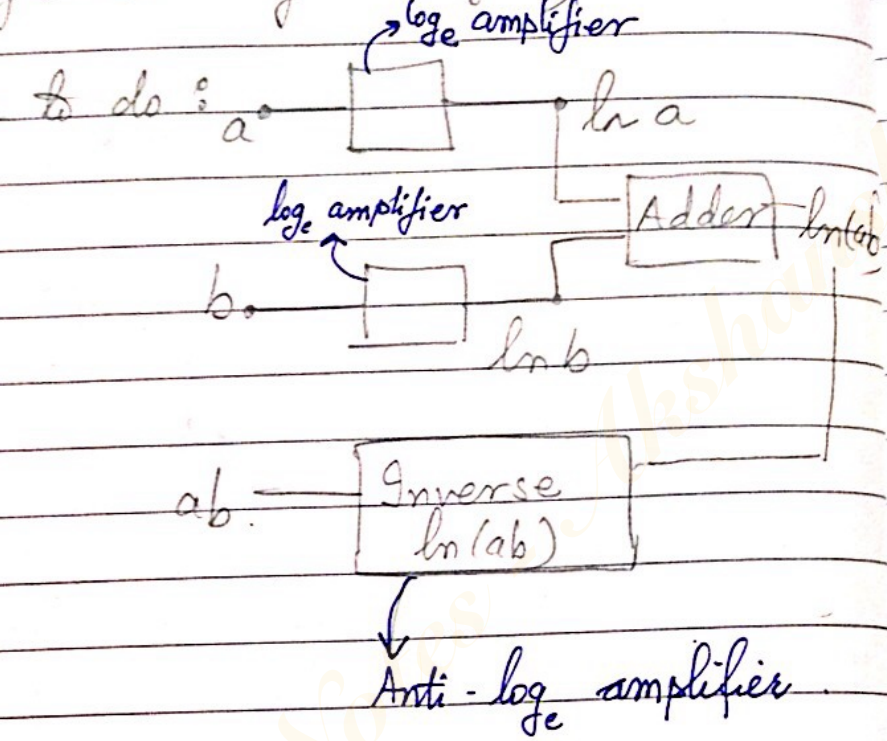
$3 \sin \omega t$ → Just give gain of 3 to $\sin \omega t$ = $3 \sin \omega t$

$4 \sin^3 \omega t$ → multiply $\sin \omega t$ by itself & again by itself.

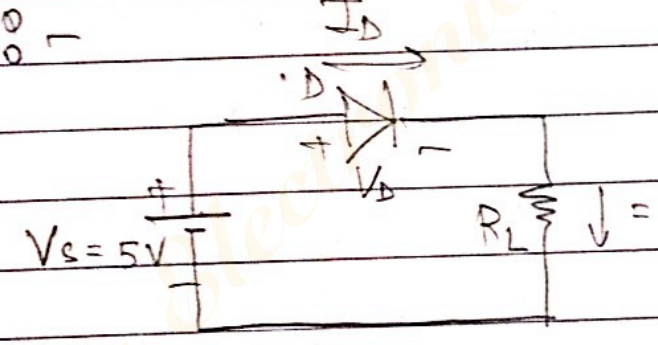
How to make op-amp as a multiplier?

Multiplic^n of 2 i/p $\equiv$ Adding log. values of 2 i/ps.

($\because \log(ab) = \log a + \log b$)



eg :-



Find V_D, I_D

KVL: $5 = V_D + I_D R_L$ → (1)

& $I_D = I_S\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right]$ → (2)

→ 10^{-14} A, will be given.

Idea:

Use method of successive approxim^n.

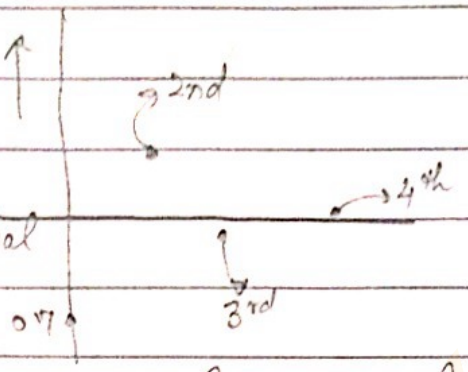
i.e, lets say $V_D = 0.7\,V$.

Use this in eq^n (1) to get I_D

Use I_D in eq^n (2) to get V_D.

Keep doing this.

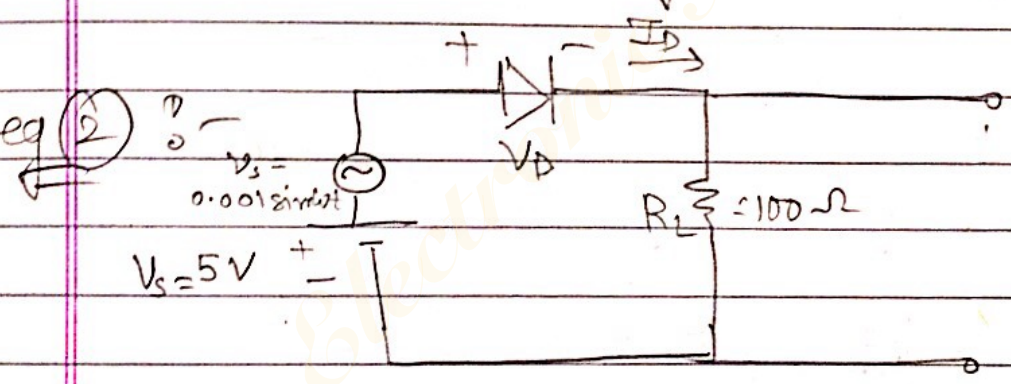
Idea (as done before) :-



If initially I assumed 0.7 & say, its lower than actual value; on the next cycle, I will get a value more than actual (closer to actual). Keep doing (till 3rd iteration) to get a closer value to actual — Done.

This is final V_D.

Use this to get I_D.



Find AC component of voltage across R_L :-

(Note : DC component, $V_L = I_D R_L$)

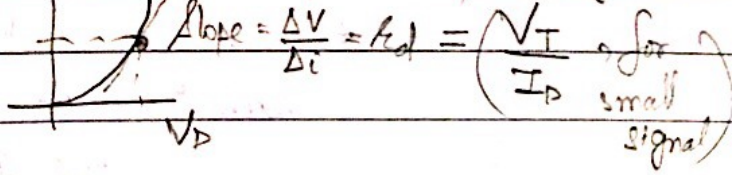
Idea :-

Draw small signal model.

↳ Kill all DC.

↳ Replace diode by its resistor equivalent

↳ resistance = Slope at operating pt.

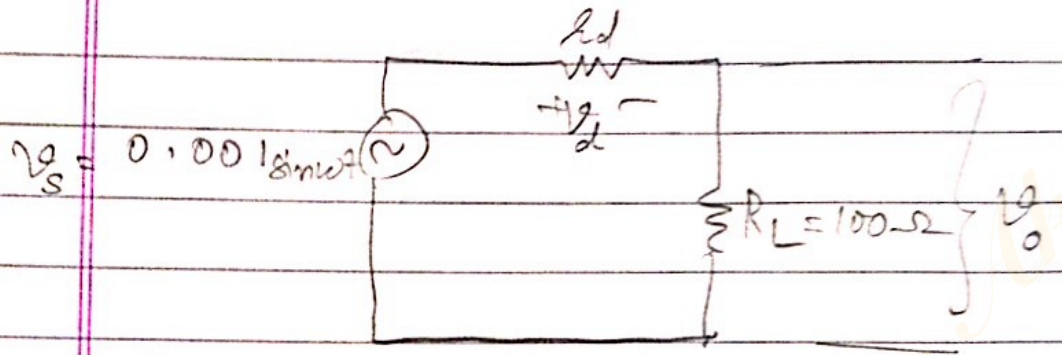


So, we have

$$r_d = \frac{0.026}{I_D}$$ ✓

I_D → from DC analysis

Small signal circuit :-

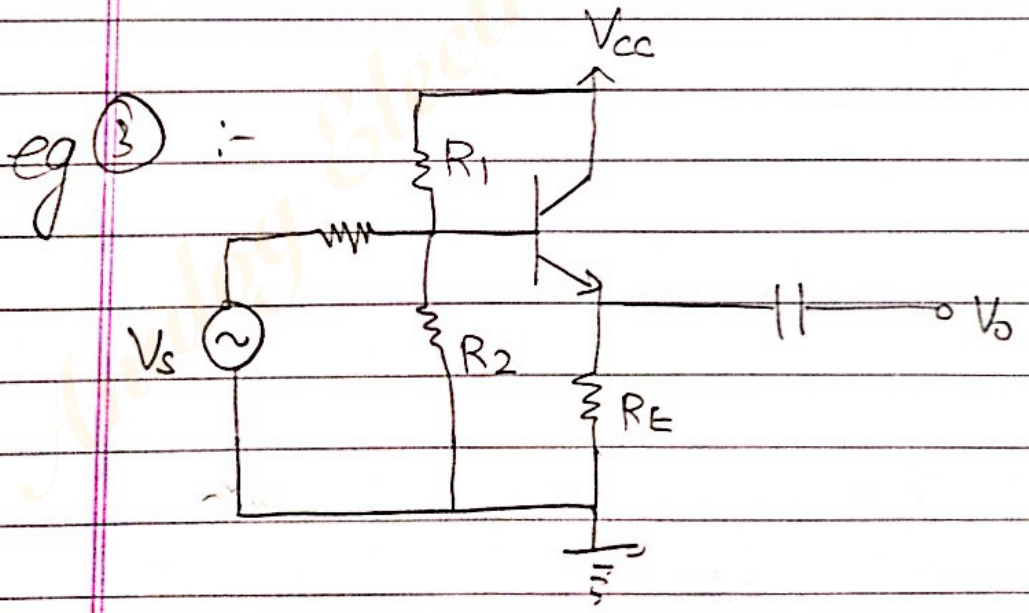


Now, o/p voltage due to signal,

$$v_o = \frac{R_L}{R_L + r_d} \times (0.001 \sin \omega t)$$ ✓

(Voltage divider rule)

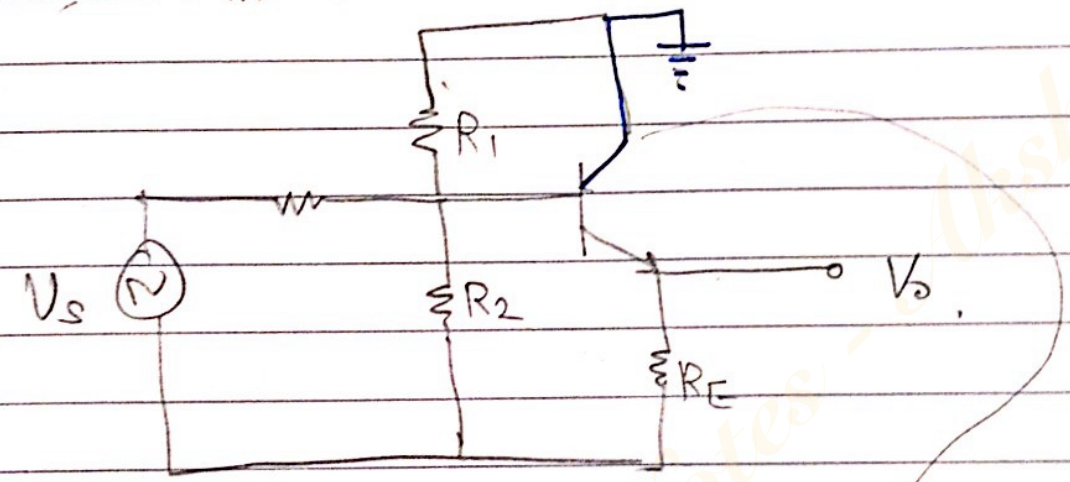
eg (3) :-



(1) See if it's CE, CC or CB Amp.

Idea : Ground DC & see amplifier's fn" for given signal (short circuit capacitor)

So, we make :-



We find, collector is common terminal here. Meaning, it's directly grounded. (No resistor in between).

So, its CC amplifier.

... continued.

Designing an OP-AMP circuit for Temperature Measurement using RESISTANCE TEMPERATURE DETECTORS (RTD)

✱ What is RTD?

- Resistance depends on temperature
- Temp. coeff > 0 for most metals.
- Metals like gold, platinum etc used

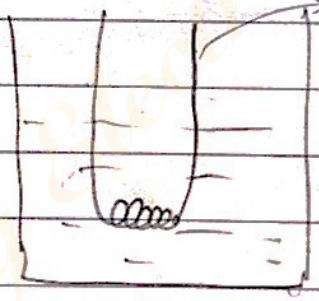
Resistance of RTD varies with temp. linearly:

$$R_T = R_0[1 + \alpha T]$$

- R_0: Resistance at 0°C
- R_T: Resistance of RTD at T°C
- α: temp. coeff (0.004 – 0.005/°C)

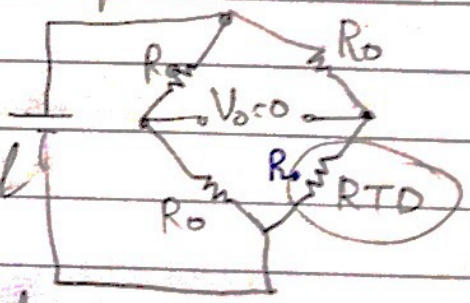
This is used in instruments as a temp. detector.

✱ Suppose I am boiling water



Resistance temperature detector

- has a Wheatstone bridge arrangement



One of the resistors is replaced with RTD. Now, when Wheatstone bridge is balanced,

$V_0 = 0$.

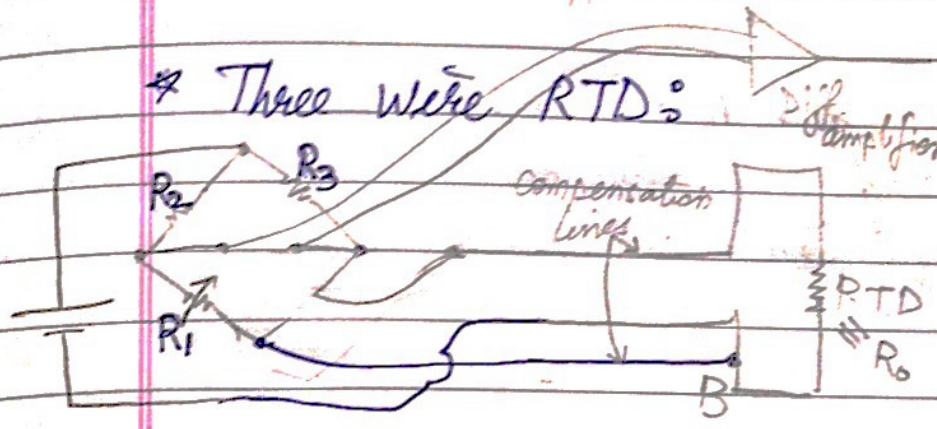
When Temp ↑, resistance changes. Hence, $V_0 \neq 0$ now. This change in voltage is read as resistance.

Now, let the change in o/p voltage = ΔV_o.

Idea:

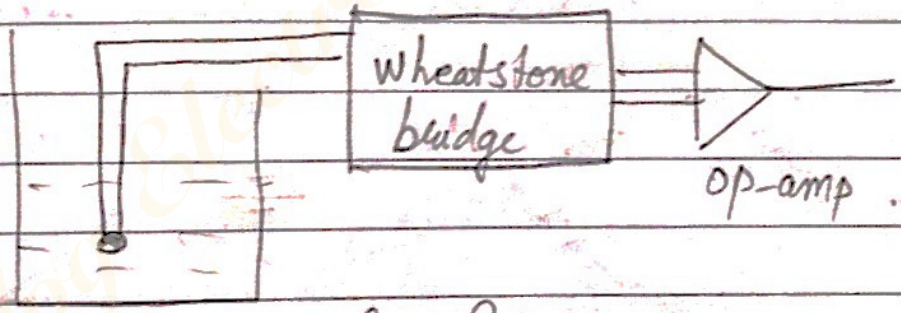
Feed in ΔV_o to a difference amplifier. Now, o/p can be recorded in temp.

* Three wire RTD:



When leads, coming from boiling water, they have some resistance. Now, when joined to wheatstone bridge, matching goes off. So, a 3rd resistance lead matches the bridge.

Q.



We want to make alarm sys. — alarm gets on when $T > T_1$, say.

Normally, $R_2 = R_3$ & $R_1 = R_0$.

Resistance associated with long wires of RTD. is also accomodated.

When $T \uparrow$, $R_1' = R_1 + X$, $R_0' = R_0 + X$

$R_1 \to R_1 + X$. So, R_0 can be changed s.t cond^n is still maintained.

Self heating in RTD

$\Delta T = P_D$ → Power dissip^n factor

↳ P: Power dissipation in RTD (W)

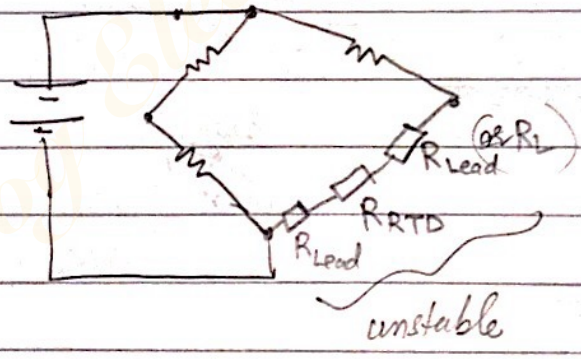
↳ ∃ some extra heating taking place in RTD. Current flowing through it causes i^2R heating. The small temp rise is ΔT

* In 3 wire RTD, 2 wires are connected across 4th resistor (replacing it). 3rd wire is connected to power supply.

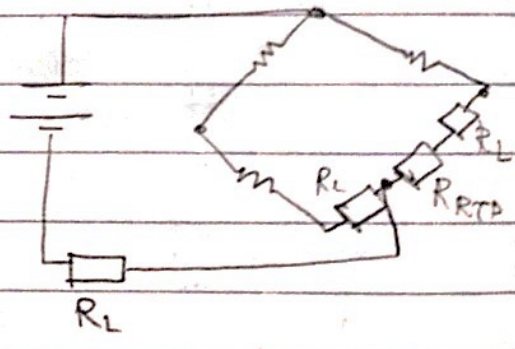
The lead resistances are appropriately connected to compensate change in resistance.

So,

2 wire RTD



3 wire RTD



*** Q. Design problem:-

Design an on/off water temp. control sys.

o/p = 0 - 2 V

Temp → 40 - 90 °C.

RTD PT-100 (3 wire type) is used

Also, an alarm should be raised when T = 95°C.

Given:-

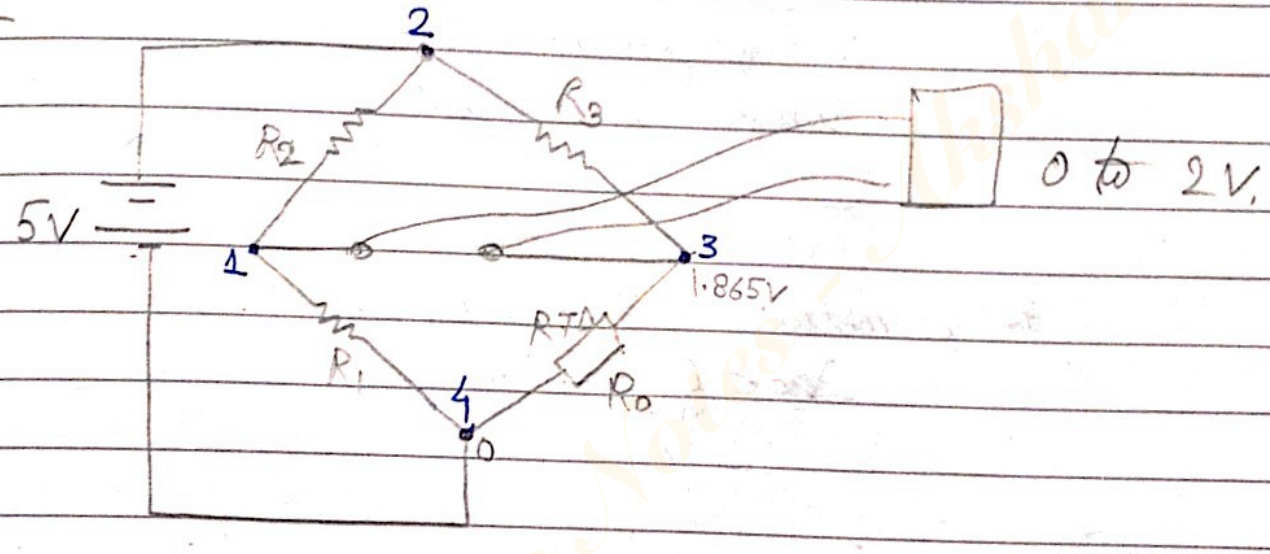
ΔT = 1°C (Temp ↑ due to self heating)

5V power supply is used for Wheatstone bridge.

P_D = 30 mW/°C.

Soln :-

Part A



Idea, we want 0V at 40°C & 2V at 90°C.

So, for 40°C, ∃ null cond^n (0V).

Now, find resistance of RTD at 40°C

$$R_T = R_0(1 + \alpha T)$$

R_0 & α got from the data sheet of product specified.

So, $R_{40} = 116\ \Omega$.

Now,

$$\Delta T = \frac{P}{P_D} \Rightarrow 1 = \frac{P}{30} \Rightarrow P = 30\ mW$$

Now, $P = I^2R \Rightarrow 30mW = I^2 \times 116$

$$\Rightarrow I_{R_{40}} = 16.08\ mA.$$

& $V_{R_{40}} = 16.08 \times 116 = 1.865\ V$

Also, Now, $\therefore V_{R_{40}} = 1.865\,V$

& node 4 is at 0 V potential.

So, potential at node 3 = 1.865 V = V_2, say

For bridge to be balanced,

$V_1 = V_2 = 1.865$.

Now, finding resistances :-

By Voltage divider rule,

$$\left(\frac{R_1}{R_1+R_2}\right) 5\,V = 1.865\,V \rightarrow (1)$$

Also, across nodes 2 & 3,

$$\frac{V_2 - V_3}{I_{R_{40}}} = R_3$$

current same across R_3 & R_0.

$$\Rightarrow \frac{5 - 1.865}{16.08\,mA} = R_3$$

$$\Rightarrow R_3 = 195\,\Omega.$$

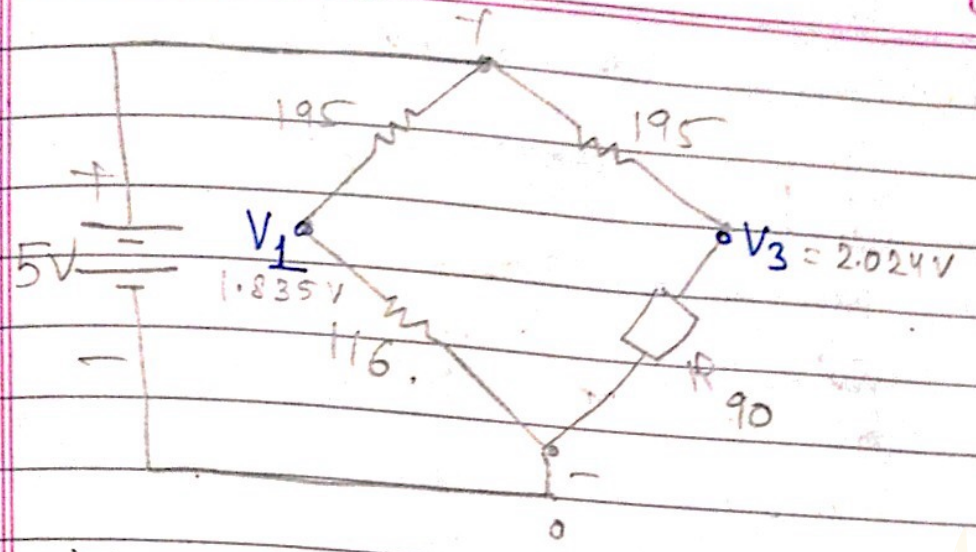
Now, again, for balancing,

$R_3 = R_2$

So, $R_2 = 195\,\Omega$.

Next, R_1 is a potentiometer. So, its resistance can be changed to make it equal to R_0 (116 Ω).

Finally, we now take T = 90°C & analyse the circuit :-



Now, $R_{90} = R_0(1 + \alpha(90))$

$\Rightarrow R_0 = 136\ \Omega$.

195 ∥ 0 = 111

Also, as R_1 & R_2 didn't change,

So, V_1 remains 1.865 V.

A problem now: We got $R_2 = R_3 = 195\ \Omega$.

195 Ω is not available. (not a standard resistor)

So, we take $R_2 = R_3 = 200\ \Omega$.

As we have done this change, V_1 becomes

$$V_1 = 1.835\,V \left[\frac{5}{1} \times \frac{116}{316}\right]$$

& $V_3 = 5 \times \frac{136}{336}$

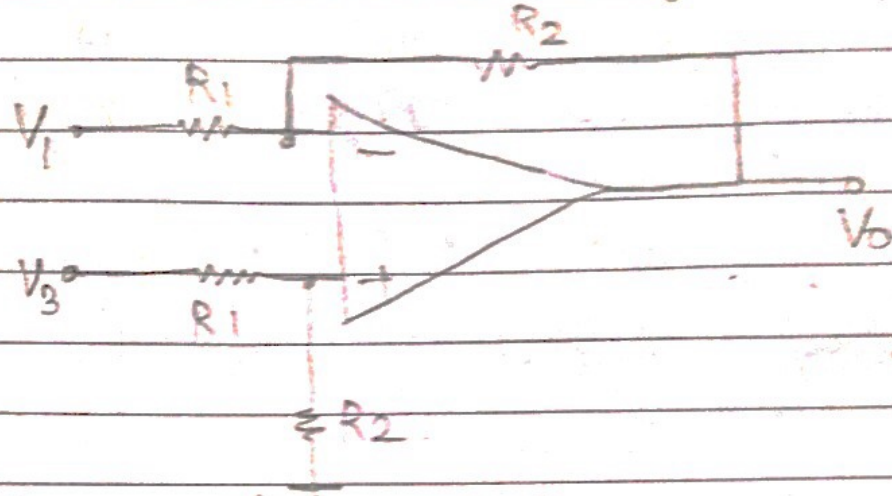
$R_1 + R_2$

So, $V_1 = 1.835$ V & $V_3 = 2.024$ V

Now, ∃ voltage diff. b/w V_1 & V_3. So, use difference amplifier to amplify this.

(PTO)

$V_3 > V_1$ So, V_2 : non inverting terminal



So, $V_o = (V_3 - V_1)\left(\frac{R_2}{R_1}\right)$

$V_o = (0.189)\left(\frac{R_2}{R_1}\right)$

We want $V_o = 2\ V$ (at 90°C)

$\Rightarrow \frac{R_2}{R_1} = \frac{2}{0.189}$

$\Rightarrow \frac{R_2}{R_1} = 10.58$

So, for designing, take $R_1 = 1k\Omega$ & $R_2 = 10.58k\Omega$

Next, in b/w 40°C & 90°C, RTD shows linear behaviour in its change of resistance $[R_T = R_0(1+\alpha T)]$.

Part-B Designing alarm:

So, at 95°C,

$R_{95} = 138\ \Omega$ & $V_1 = \frac{5 \times 116}{316} = 1.835\ V$

& $V_3 = \frac{5 \times 138}{338} = 2.041\ V.$

★ Note: Comparators dont have -ve feedback.

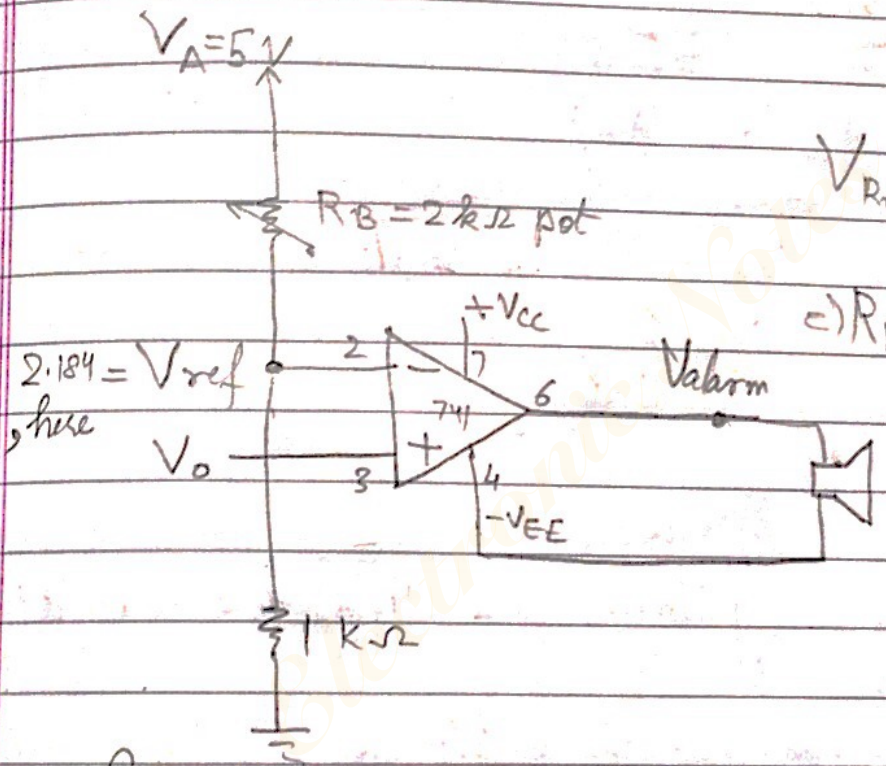
So, $V_3 - V_1 = 0.2064$ V. (So, changed from 0.189 → 0.2064)

Now, op amp o/p = $10.58 \times 0.2064 = 2.184$ V.

When o/p reaches 2.184 V (from 2 V) we should get buzzer sound.

Idea:

Use COMPARATOR.



$V_{Ref} = 2.184 = \frac{5}{1 + R_B}$

$\Rightarrow R_B = 1.29$ kΩ.

(Adjust pot to this value)

When $V_o < V_{ref}$, $V+ < V-$

So, o/p = $-V_{cc}$.

So, buzzer doesn't sing.

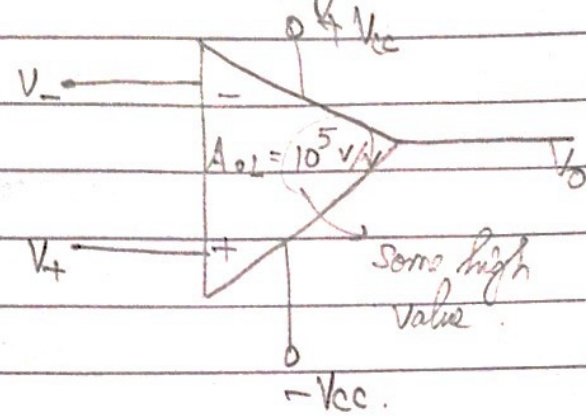
When, $V_o > V_{Ref}$, $V+ > V-$

So, o/p = $+V_{cc}$.

Buzzer sings.

✡ PRACTICAL OPERATIONAL AMPLIFIERS.

↳ Open loop gain, A does not tend to ∞.



For ideal op-amp,

$V_o = A_{OL}(V_+ - V_-)$

↳ $A_{OL} \to \infty$.

So, for V_o to be finite, $V_+ = V_-$

Note: V_o cannot exceed V_{cc}.

So, if $V_+ - V_- = 0.0001$

Then, $V_o = +15$ V $(+V_{cc})$

& if $V_+ - V_- = -0.0001$

Then, $V_o = -15$ V $(-V_{cc})$

Now, because gain is still very high, So, V_+ is considered very close to V_-

how close? →

I want V_o to be either ± 15 V & $A_{OL} = 10^5$.

So, $\pm 15 = (V_+ - V_-) \times 10^5$.

$\Rightarrow V_+ - V_- = \frac{\pm 15}{10^5}$

So, the diff. that can be taken b/w V_+ & V_- = 0.15 mV.

Gain in dB = $20 \log(A_{OL})$
$= 20 \log(10^5) \simeq 100$

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* typically, value of open loop gain is 80-120 dB.

- Input resistance
  - ↳ For differential i/p, i/p resistance (Rid) → small
    common mode i/p, R_{ic} → large.

- Output resistance
  Ideally = 0
  Practically → finite (but non zero)

- CMRR (Common mode rejection ratio)
  large but not infinite.

- i/p offset voltage and bias currents.

Offset: Non zero but typically small values.
Ideally: If $V_{in} = GND = 0$, ∃ no o/p.
Practically: V_o = finite.
↳ Why not ideal?
We assume both differential amplifiers (lying inside OP-AMP) are identical. But, ∃ some difference. So, even if i/p = 0, ∃ some change & we get some o/p.
This is accounted for by OFFSET

Bias currents: We assume $i_+ = i_- = 0$ (i.e., no current goes to base). But practically, something goes. So, changes behaviour & values.

Now, we saw that we gave $V_+ = V_- = 0$.
We expected $V_o = 0$ ∴ But we got some V_o
Now, to model that .. we add 3 things to ideal amplifier (op amp) ⟶ i_+, i_- & V_{oc}

- **Slew rate :** (SR)

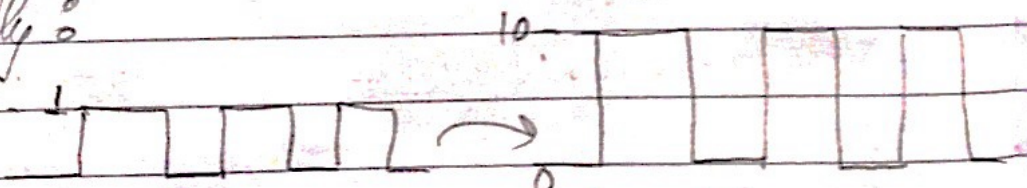
  Now, we expect a sinusoidal i/p to give same sinusoidal o/p. (same ≡ same phase).
  Now, practically, ∵ ∃ some active devices in between, ∃ some delay in the circuit.
  So, o/p voltage's sinusoid is delayed as compared to i/p.

$$SR = \left(\frac{\Delta V_o}{\Delta t}\right)_{max}$$ for a step change in input.

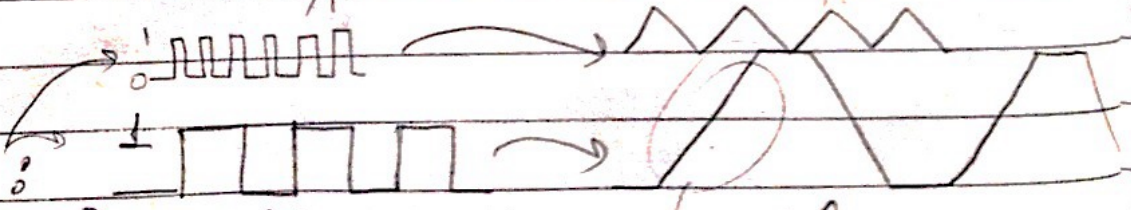
↳ max. time with which signal can change. So, if i/p is supplied with a very high freq, o/p may lag behind the i/p.

Graphically :

Ideal :-

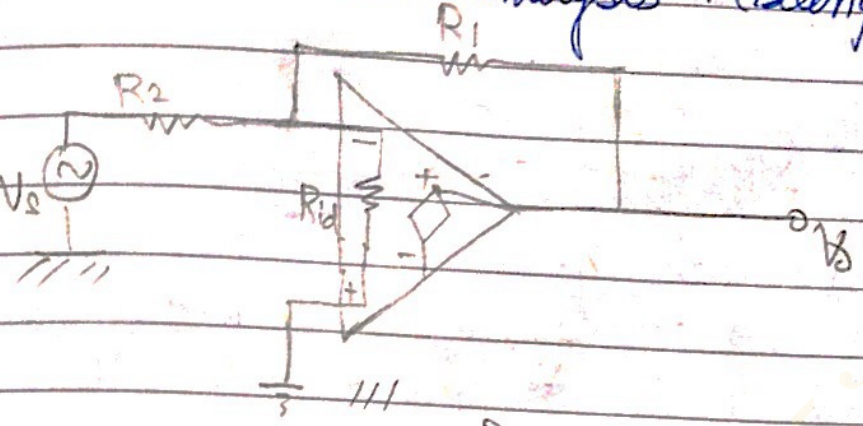


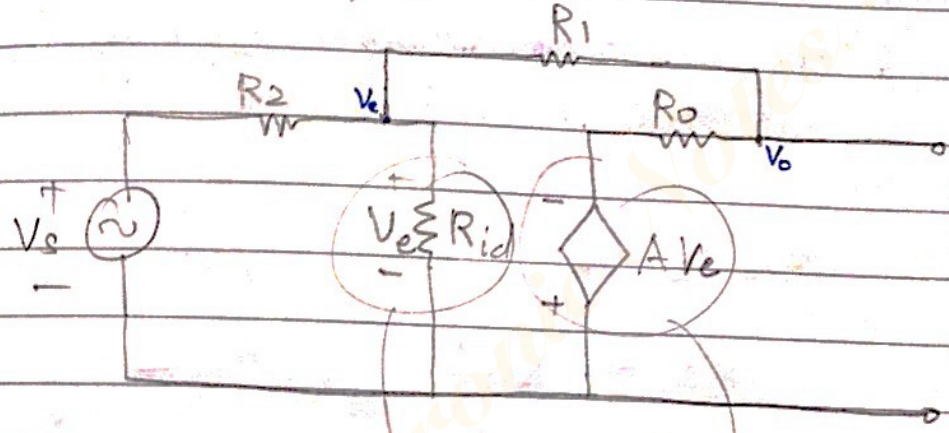
Practical :



* If i/p freq. is very high, Δ triangular waveform

* • Non-Ideal OP-AMP Analysis :- (Seeing finite gain)





→ additional i/p resistance (Previously → ideally was infinite)

Adding a dependent voltage

Now,

$V_o = -A V_e + I(R_o)$ → 0 ; $\frac{V_s - V_e}{R_2} = \frac{V_e - V_o}{R_1}$

Note : We take $R_{id} \to \infty$. So, I across $R_{id} = 0$

$$A_v = \frac{V_o}{V_s} = \left(-\frac{R_1}{R_2}\right)\left(\frac{A\beta}{1+A\beta}\right)$$

→ Additional factor

↳ $\beta = \frac{R_2}{R_1 + R_2}$ = Feedback factor

↳ effect of R_o has been neglected.

In ideal, we get $A_v = (-R_1/R_2)$. So, it has changed.

Was ideally infinite. Now, finite ← Open loop gain of op-amp

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- in most practical op-amps, $A\beta >> 1$.

So, $A_V \simeq -\left(\frac{R_1}{R_2}\right)$

↳ same as of ideal

In ideal op-amps $\therefore A\beta \to \infty$.

$\Rightarrow A_{V_{ideal}} = -\frac{R_1}{R_2}$

So, we can write :-

$$A_r = \frac{V_o}{V_s} = A_{V_{ideal}} \left(\frac{A\beta}{1+A\beta}\right)$$

$$\simeq A_{V_{ideal}} \left(\frac{A\beta}{A\beta}\left(\frac{1}{1+1/A\beta}\right)\right)$$

$$\simeq A_{V_{ideal}} \left(\frac{1}{1+1/\alpha}\right)$$

↳ $\alpha >> 1$

$$\Rightarrow A_V \simeq A_{V_{ideal}} \left(1 - \frac{1}{\alpha}\right)$$

$$\Rightarrow A_V \simeq A_{V_{ideal}} \left(1 - \frac{1}{A\beta}\right)$$

If A changes, A_V will change

$$\text{Figure of merit} = \frac{\Delta A_V}{A_V} = \frac{A_{V_{ideal}} - A_V}{A_V} = \left(\frac{1}{A\beta}\right)$$

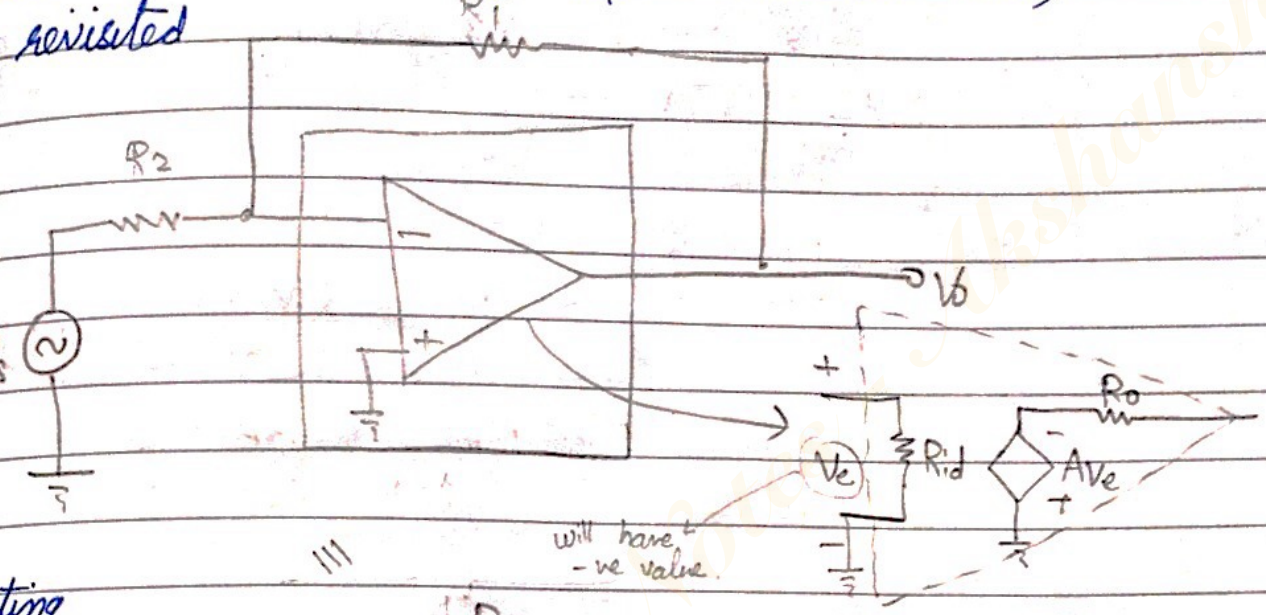
↳ Now we want $1/A\beta$ as small as possible. So, always choose op-amp with large value of A (and/or large value of β)

* In practical op-amps, $A \simeq 10^5$

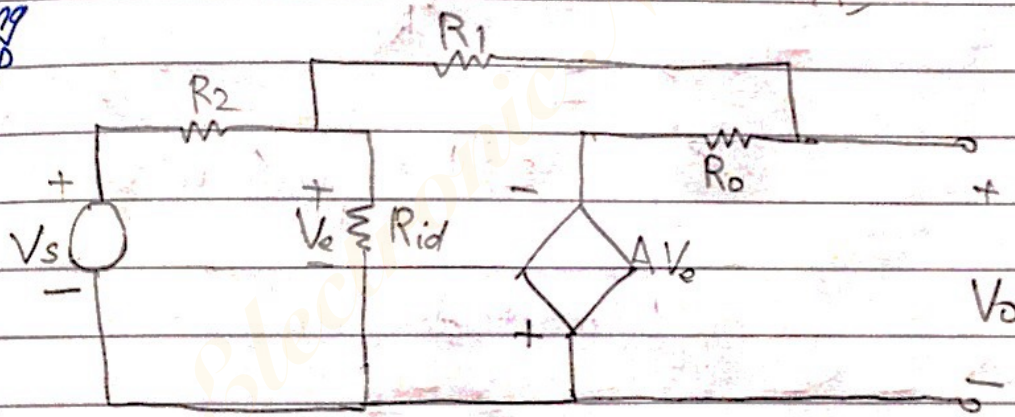
Ideally, $\frac{\Delta V}{A} = 0$; $\because A \to \infty$,

* Non-Ideal OP-AMP : Seeing Input Resistance (R_{in})

Circuit revisited

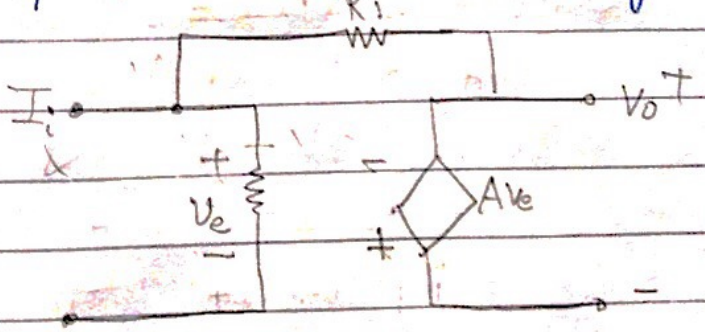


Inverting op-amp



(Note : had it been an ideal op-amp, $R_{id} \to \infty$ (OC) & $R_o \to 0$ (SC))

here, for simpler treatment, neglect R_o.



Finding i/p resistance:

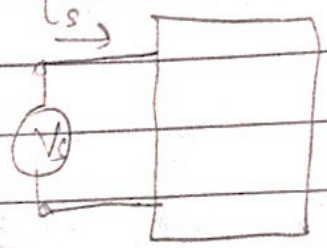
See it as a 2 port network

Apply source → V_s & measure current I_s.

$$\frac{V_s}{i_s} = R_{in}$$

R_{in} → i/p of op-amp

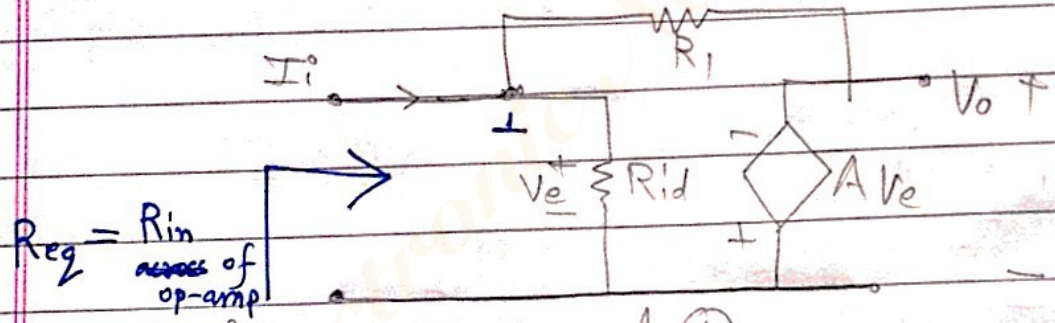
→ i/p of circuit



For i/p of op-amp, ignore R_2

So, current, I_i enters op-amp +ve part of OP-AMP.

Note: We also consider current flowing through +ve part of OP-AMP.



Applying KCL at node ①,

$$\Rightarrow I_i = \frac{V_e}{R_{id}} + \frac{V_e - V_o}{R_1}$$

Now, Ignoring R_o, $V_o = -AV_e$

$$\Rightarrow I_i = \frac{V_e}{R_{id}} + \frac{V_e - (-AV_e)}{R_1}$$

$$= \frac{V_e}{R_{id}} + \frac{(1+A)V_e}{R_1}$$

$$\Rightarrow I_i = V_e\left[\frac{1}{R_{id}} + \frac{1+A}{R_1}\right]$$

$$\Rightarrow R_{eq} = \frac{V_e}{I_i} = \left[\frac{1}{R_{id}} + \frac{1+A}{R_1}\right]^{-1}$$

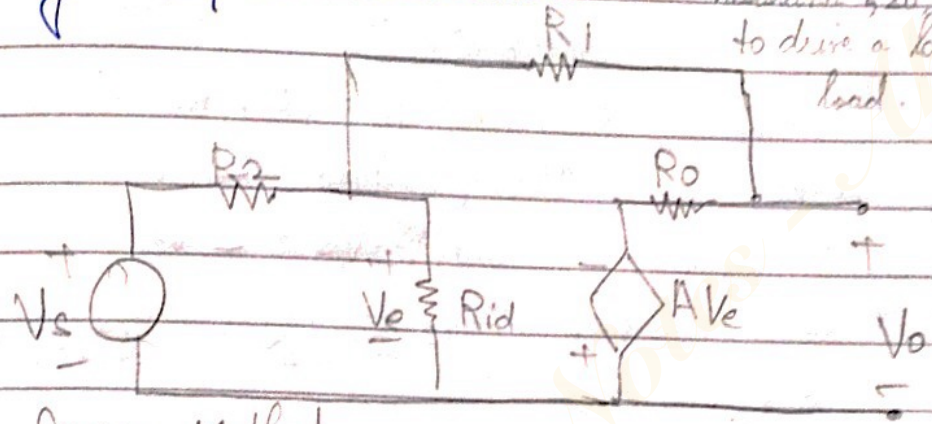
So, R_{in} of circuit = R_{in} of op-amp (R_{eq}) + R_2

$\Rightarrow R_{in} = R_{eq} + R_2$

$\Rightarrow R_{in} = \left(\frac{1}{R_{id}} + \frac{1+A}{R_1}\right)^{-1} + R_2$

✱ Seeing Output Resistance

→ i.e., op-amp, itself having some resistance, so we'd be able to drive a low resistance load.



Test Source Method.

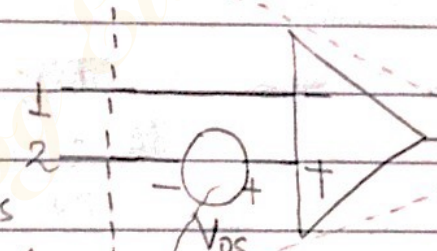
Apply test source at o/p (V_x, having current I_x)

Now, remove V_s & find $\frac{V_x}{I_x} = R_o$ ✓

✱ DC Offset Voltage, V_{os}

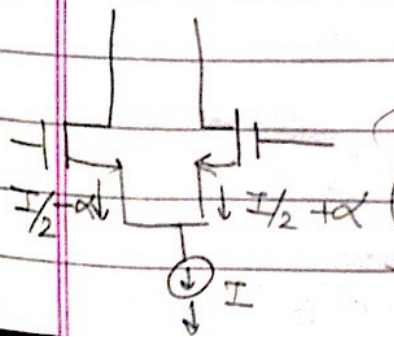
V_{os} is the DC offset voltage that makes $V_o \neq 0$, when V_1 & V_2 are grounded

∃ offset if the 2 transistors are not identical



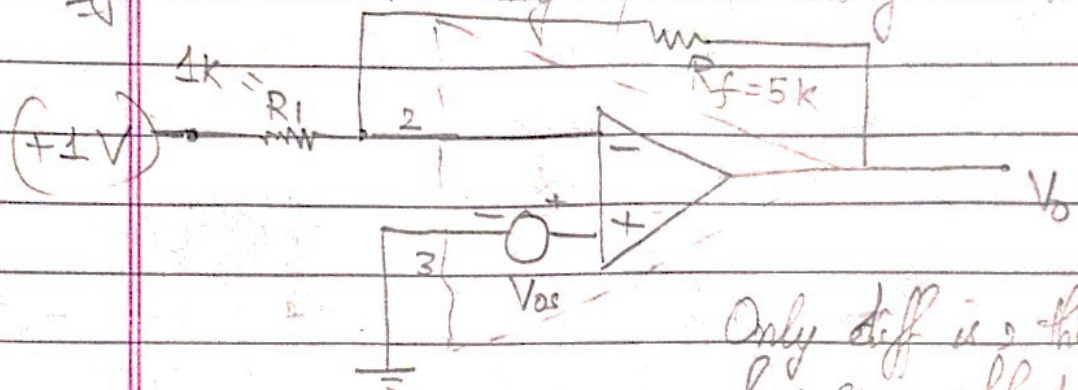
→ Adding V_{os} to non inverting terminal of an otherwise ideal op-amp.

→ V_{os} can be +ve or −ve depending upon the diff b/w i/p voltage of 2 transistors



→ Small change at differential stage gives high change at the end of differential stage (o/p)

eg: Construct inverting op-amp using non ideal op-amp



Only diff is, this op-amp has some offset voltage.

Now, find V_o, if $R_1 = 1k$, $R_f = 5k$,

$V_{os} = 1mV$

$V_s = 1V$

It like 2 i/p voltages.

So, use POS.

Taking V_1 into account

$$V_{o1} = \left(-\frac{5}{1}\right)(1) = -5V.$$

Taking V_{os} into account

$$V_{o2} = \left(1 + \frac{5}{1}\right)(1mV) = 6mV.$$

So, $V_o = V_{o1} + V_{o2} = -4.994\ V.$

Ans

✱ Input Bias Current

↳ Property of gate oxide in the mosfet.

Oxide, very good insulator.

Any voltage applied at gate, $I_{gate} = 0$

Ideally, Resistance of oxide $\to \infty$

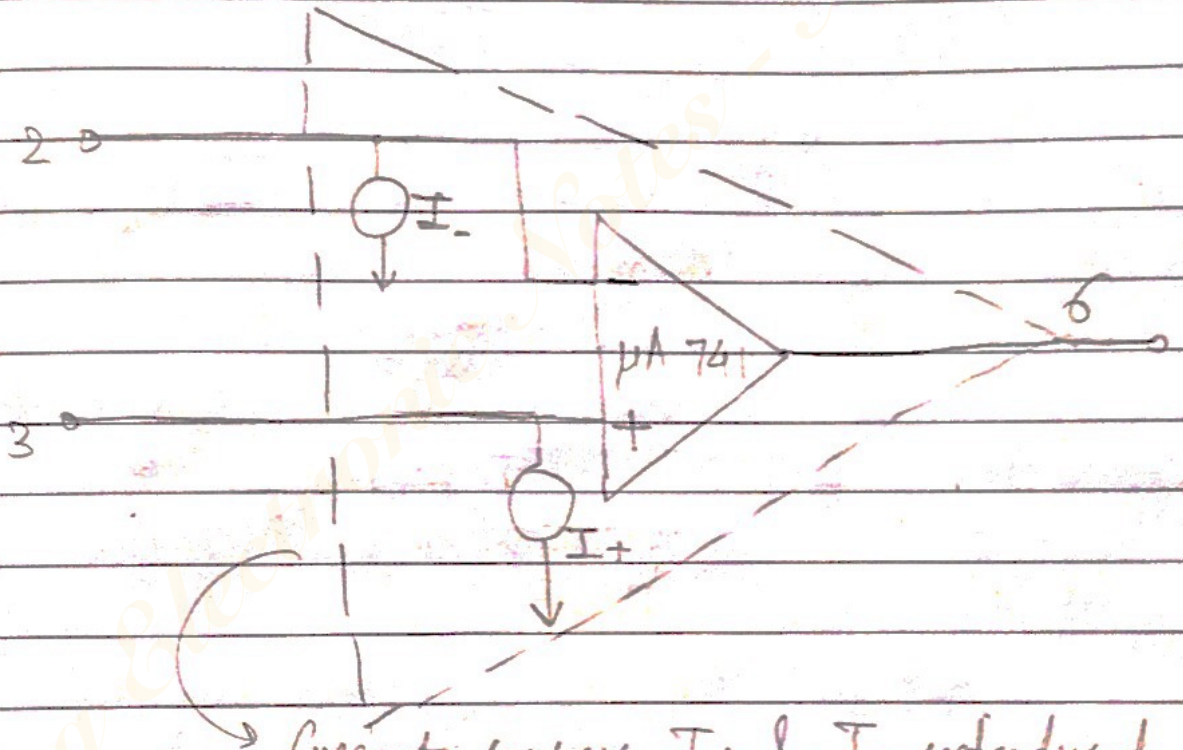
But, oxide can have some very high value, leading to some value of gate current (I_+, I_-)

(Note: For BJT, base currents are higher, so, problem is more than MOSFET)

Now, I_+ & I_- can vary. So, to model it, we take one current

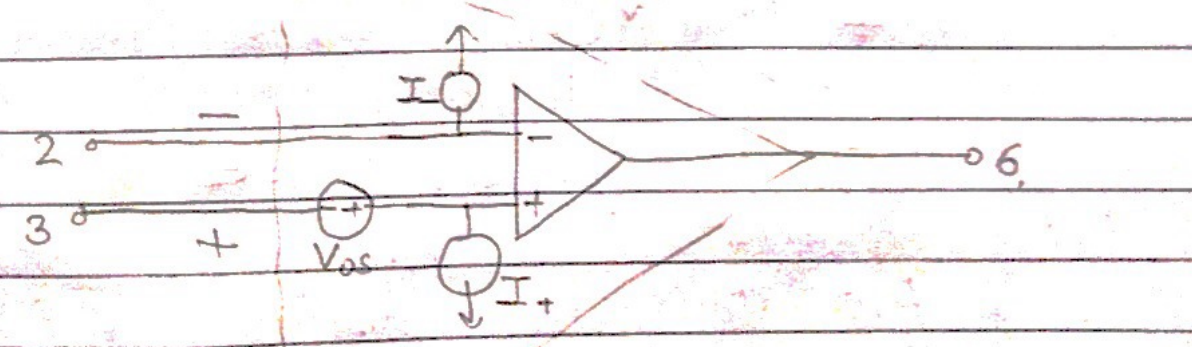
$$I_{bias} = \frac{(I_+) + (I_-)}{2}$$

As in model 5-



Current sources I_+ & I_- introduced

Adding DC offset voltage i.e., Seeing all offset together



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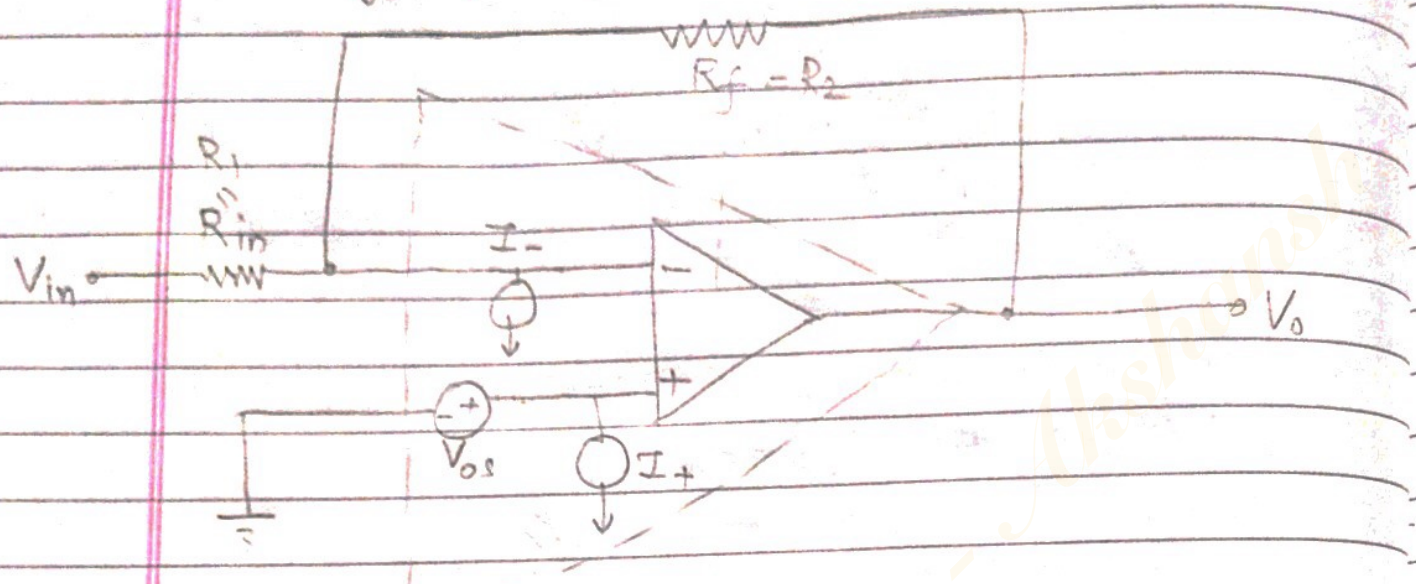
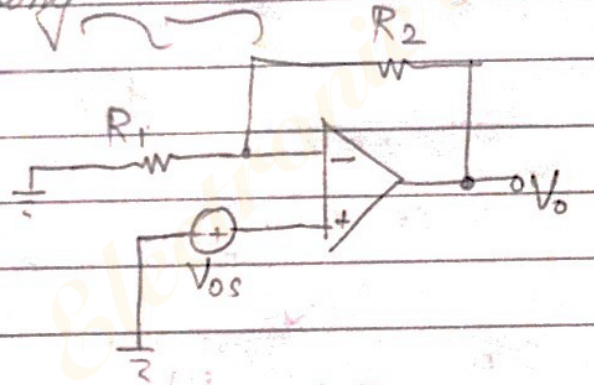
Inverting op-amp with all effects together :



The above circuit has 4 sources
↳ V_{in}, V_{os}, I_+, I_-

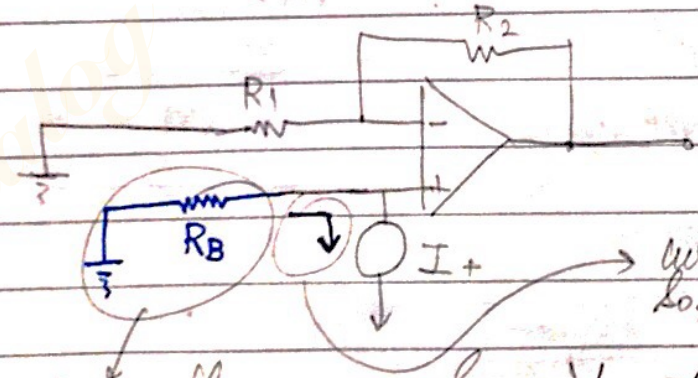
Using POS

① effect of V_{os}



$$V_{o(os)} = \left(1 + \frac{R_2}{R_1}\right) V_{os}$$

② effect of I_+



$$V_{o(I_+)} = \left(1 + \frac{R_2}{R_1}\right)(-I_+ R_B)$$

Current flows in this part. So, it has to have some resistance. let it say, has R_B.

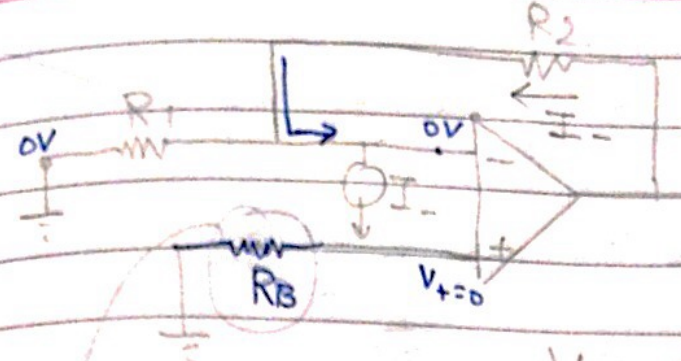
current through R_B is in → direction
So, higher potential = 0. So, lower pot. = $-I_+ R_B$

So, $V_+ = 0 - I_+ R_B$.

So,

$$V_{o(I_+)} = \left(1 + \frac{R_2}{R_1}\right) V_+$$

(3) effect of I-



Although R_B is not in use as it was there before. (Although it has no use here)

$V_+ = 0$

For ideal, $V_+ = V_-$

$\Rightarrow V_- = 0$.

$\Rightarrow R_1$ is b/w GND & 0V.

So, Current through $R_1 = 0$.

So, current in I- is only coming from feedback.

So,

$$V_{o(I-)} = I_- R_2$$

(Note : V_o is at higher potential)

(4) effect of V_{in}

Circuit is ideal, without effects.

So, $V_{o(V_{in})} = -\frac{R_2}{R_1}$ (same as before)

So,

$$V_{o(Total)} = V_{o(V_{os})} + V_{o(I_+)} + V_{o(I_-)} + V_{o(V_{in})}$$

Now, In V_o, effect of V_{os} cannot be changed. But, $V_{o(I_+)} = -ve$ & $V_{o(I_-)} = +ve$.

So, I a chance that we can remove effect due to current. For that, $V_{o(I_+)} = V_{o(I_-)}$

i.e :-

$$I_{offset} = -(I_+ R_B)\left(1 + \frac{R_2}{R_1}\right) + I_- R_2$$

$$= (I_-) R_2 - I_+ R_B \left(\frac{R_1 + R_2}{R_1}\right)$$

Now, if we make $R_B = \frac{R_1 R_2}{R_1 + R_2} = R_1 \| R_2$

$$\Rightarrow I_{offset} = (I_-) R_2 - I_+ \left(\frac{R_1 R_2}{R_1 + R_2}\right)\left(\frac{R_1 + R_2}{R_1}\right)$$

$$\Rightarrow I_{offset} = R_2 (I_- - I_+)$$

Now, usually, we take a common value of current (as seen before : $I_{bias} = \frac{I_- + I_+}{2}$)

So, $I_+ = I_-$

So, we get $I_{offset} = 0$.

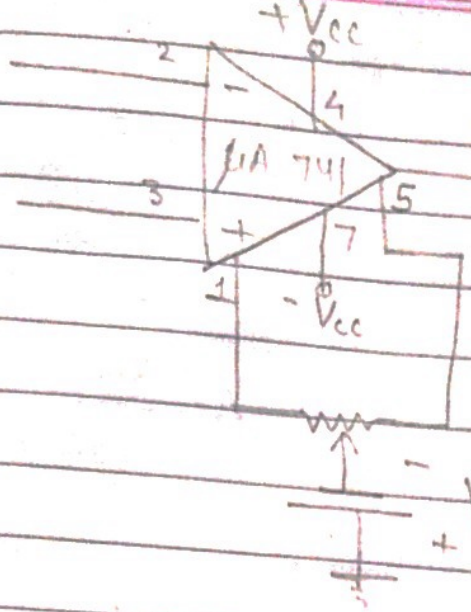
Hence, we removed offset due to current.

* Note : In prev. fig, o/p voltage for inverting op-amp doesn't depend on resistance at non inverting terminal (R_B). Now, for ideal op-amps, it's not needed, but for practical op-amps, R_B can counter bias current effect

* Offset Balancing Network.

Idea : Ideally, for 0 i/p, we should get 0 o/p. But, suppose o/p $\neq 0$, then the additional Vcc (connected) will make that o/p = 0.

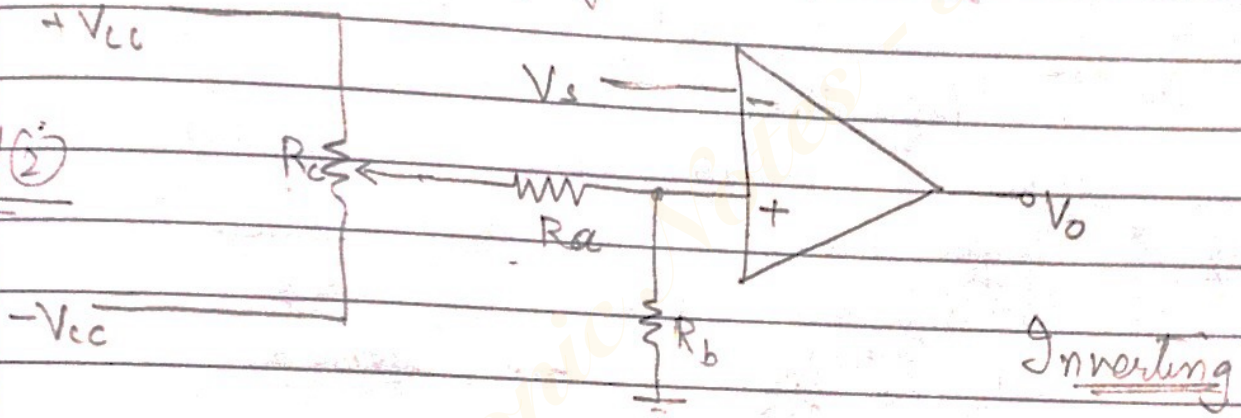
☆ Alter :-



Method ①

Inverting

Figures at bottom highlight the offset. (Circuit is incomplete



Method ②

Inverting

eg : If in above fig : $R_a = 90\,K$

$R_b = 10K$

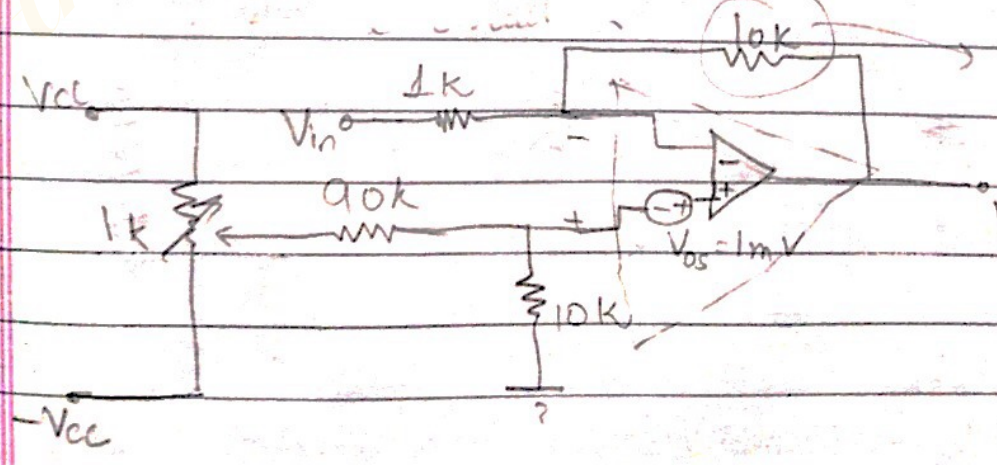
$R_c = 1K$ Pot.

Find : Circuit s.t gain = 10

op-amp has $V_{os} = +1mV$

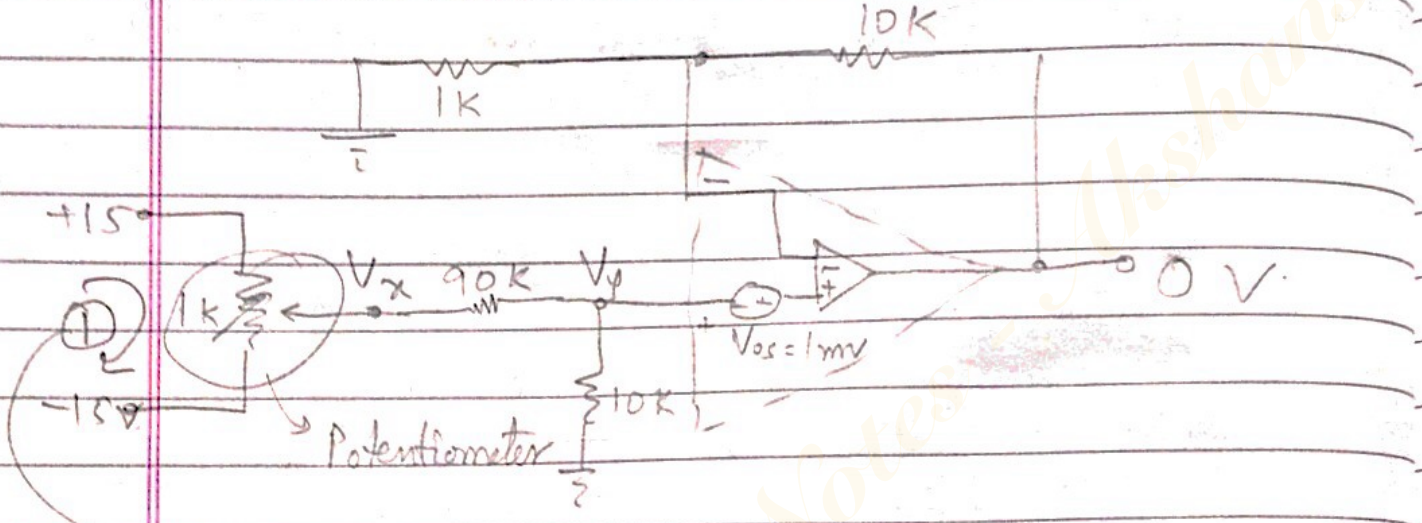
$\pm V_{cc} = \pm 15\,V$.

Ans :



Now, for getting gain = 10, consider effect of Vos (= 1mV) Now, using pot (1K), change its resistance so that it gives −1mV to cancel its effects

POS : Ground Vin. & see



Current across this branch = $\frac{30\ V}{1K}$ = 30 mA → (1)

Now, V_y = −1 mV, desired

$= \frac{10}{100} \times V_x$

$\Rightarrow V_x = -10\,mV$. (we need V_x = −10 mV to get V_y = −1 mV)

Now, to get V_x = −10 mV

$V_x = (3mA \times R) = 10\,mV$

$\Rightarrow R = 0.3\,\Omega$

Now,

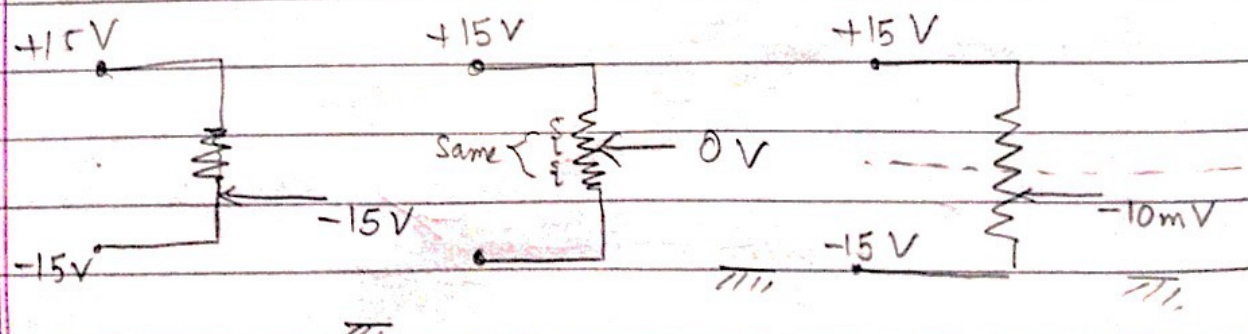


fig (1) fig (2) fig (3)

Previous fig. shows that keeping resistor (pot) a little below the middle, can give a -ve value of voltage across potentiometer (wrt ground)

Now, we want voltage across resistor = -10 mV (V_x)

&, current going through loop (1) is 30 mA

So, Voltage drop across potentiometer is (30 mA) R

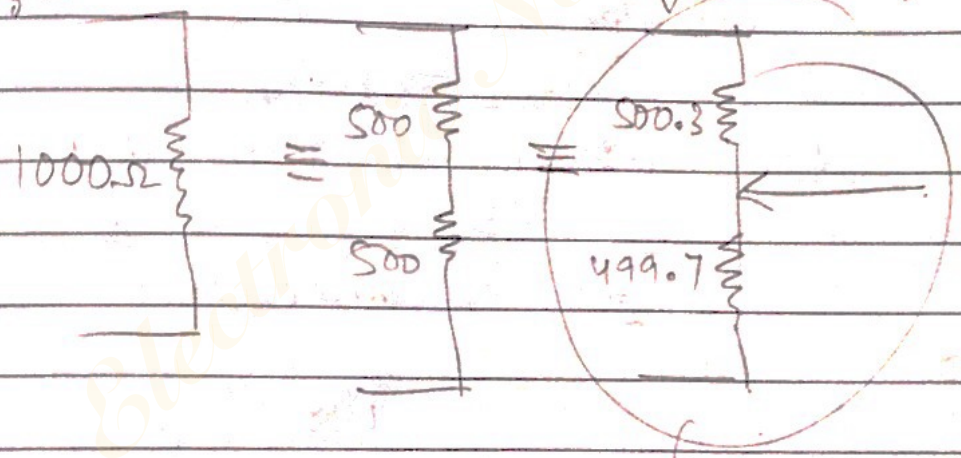
Now,

$(30\,mA) \times R = -10\,mV$

$\Rightarrow R = (-0.3\,\Omega)$

, So, go down from middle

Idea :-



If we do this, we get effect due to Vos, removed

Why use capacitors

* We use BJT in DC condition. Now, if i/p has DC voltage, we need to remove it, otherwise, it interference with DC condⁿ.

✱ FREQUENCY RESPONSE & FREQUENCY COMPENSATION IN OP-AMPS.

✱ Note : Consider BJT's

It consists of Blocking capacitors

Impedance (for capacitance)

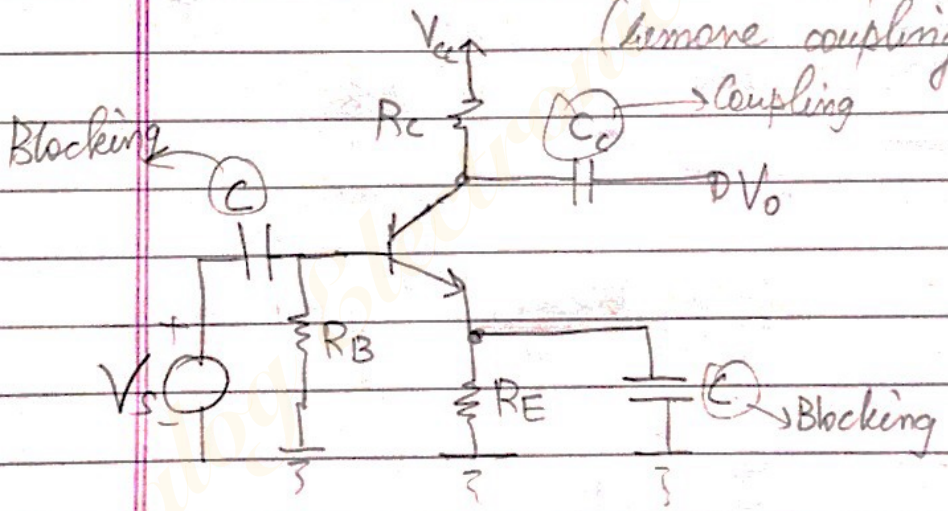
$$X_c = \frac{1}{\omega C} \cdot \text{(Reactance)}$$

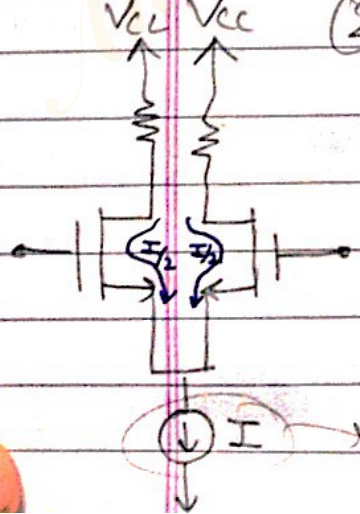
↳ for lower frequency, X_c is very high.

So, signal has a large drop across capacitor. So, it will block the i/p signal

How to prevent this gain reduction?

① Idea : Use direct coupled amplifiers (remove coupling capacitor, C)





② Idea : Use differential pair configuⁿ (Biasing is done at (I). So, I can even give DC, at gate)

Now, as drop is not there in this, so, it has high gain

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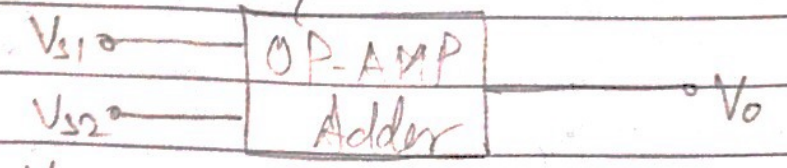
Consider op-amp inverting adder circuit :

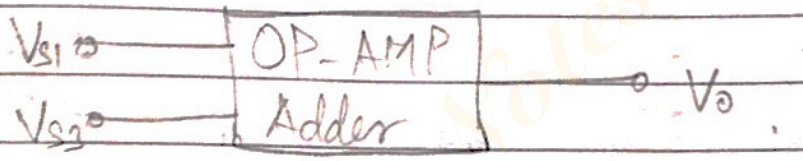
Using DC :- → Circuit as done before.



Eg $V_{S1} = 1V$, $V_{S2} = 3V$.

$V_o = 4V$, we get that

Using AC :



$V_{S1} = 1 \sin \omega t$

$V_{S2} = 3 \sin \omega t$

Now, we don't get

$V_o = V_{S1} + V_{S2}$

Why? → ∃ instantaneous addition, be it AC or DC.

So, ∃ some phase difference when adding V_{S1} & V_{S2}

☆ FEEDBACK AMPLIFIERS

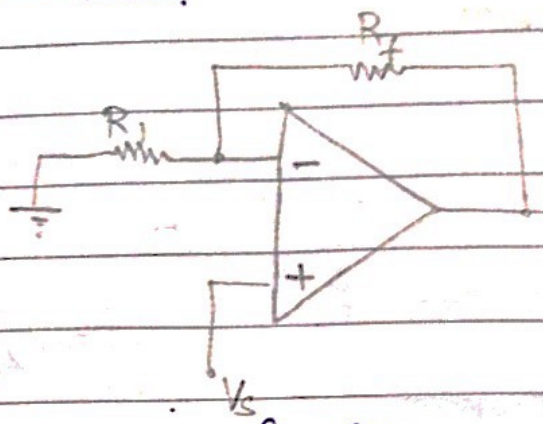


fig (1)

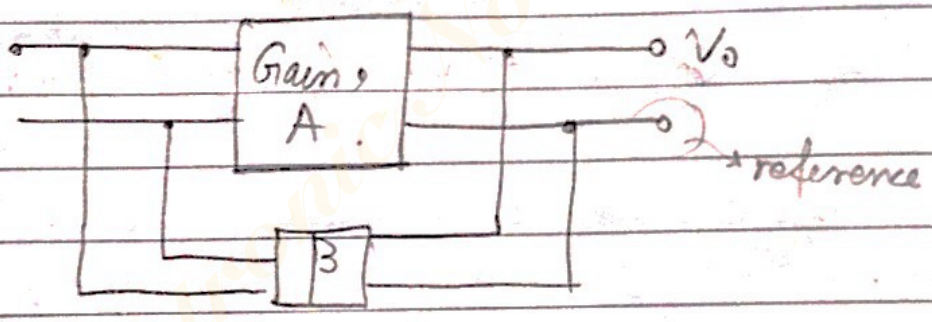
$$V_s = \frac{R_1}{R_1+R_f} \cdot V_o$$

$$\therefore \frac{V_o}{V_s} = \frac{R_1+R_f}{R_1}$$

$$\Rightarrow A_{vf} = \frac{V_o}{V_s} = 1 + \frac{R_f}{R_1}$$

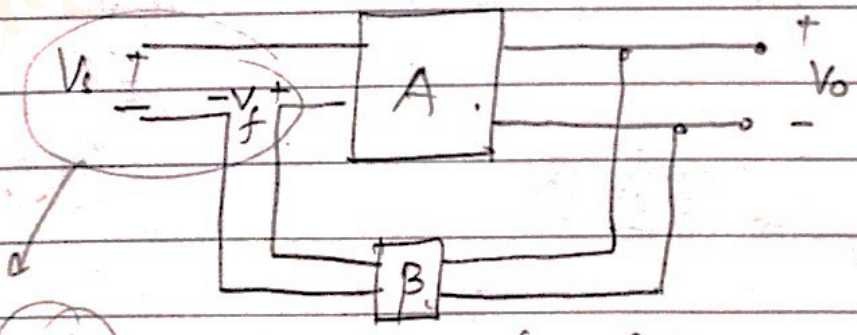
*feedback ..

Note : If ∄ no feedback, applying i/p gives o/p saturated to $\pm V_{cc}$.



↳ Shunt mixing.

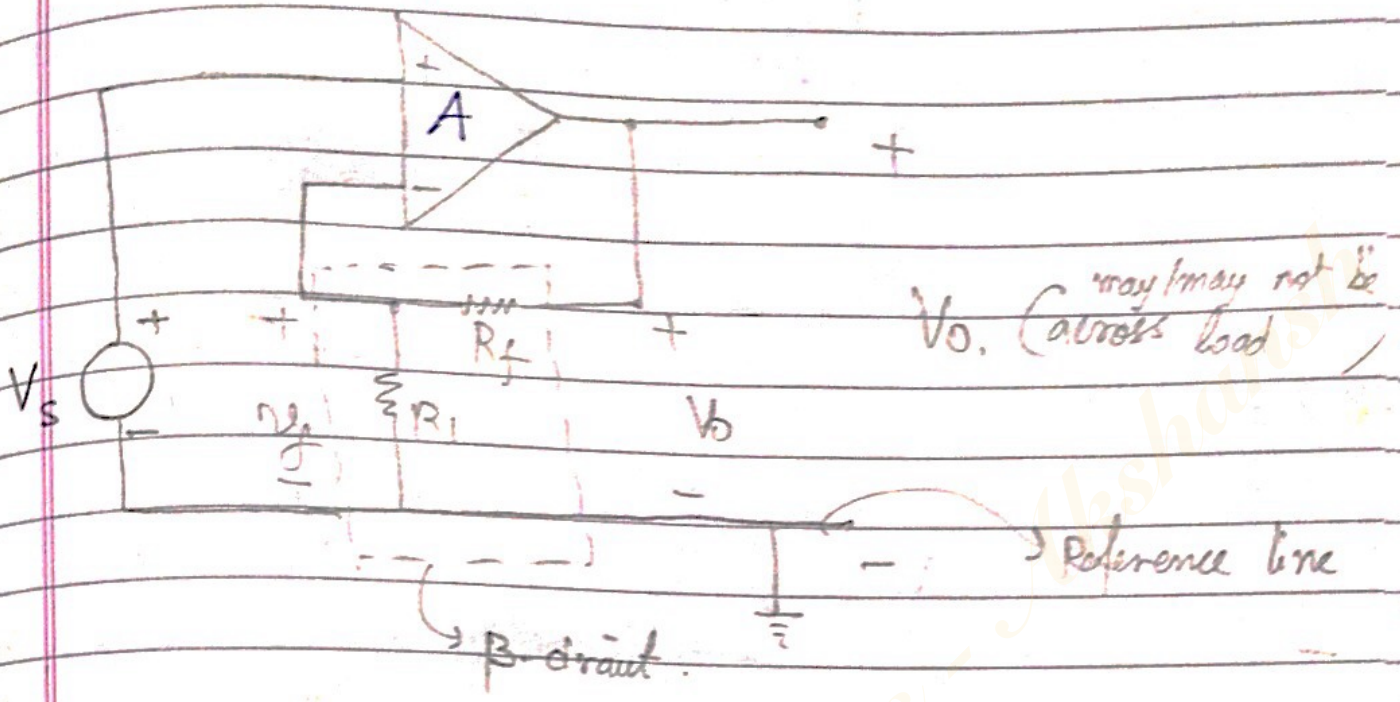
Sampling : at o/p
Mixing : at i/p.



$V_s - V_f$
↳ -ve feedback.

↳ Series mixing.

Representing fig (1) :-



It is: series mixing, shunt sampling

So, Series Shunt amplifier.

Sampling voltage (across load) & mixing in series (the voltage) ⇒ It a VOLTAGE Amplifier ★

So, gain = $A = (V/V_i)$

Now, $A_f = \frac{A}{1+A\beta}$ → Open loop gain

Feedback gain → $\beta = \frac{R_1}{R_1+R_f} \left(= \frac{V_f}{V_o}\right)$

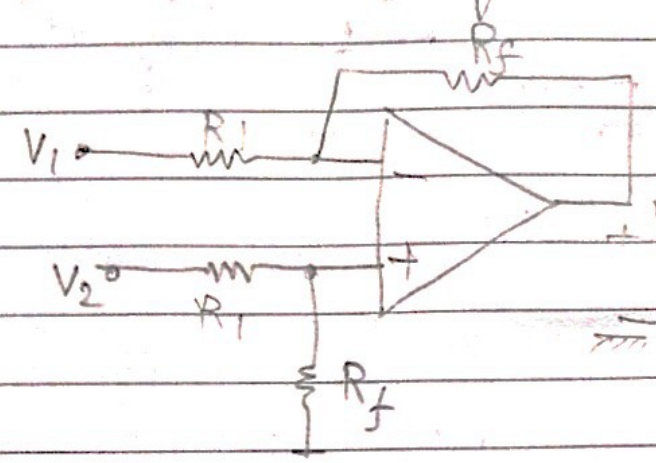
So, $A_{v_f} = \frac{1}{1/A + \beta}$

↳ for $A \to \infty$.

$\Rightarrow A_{v_f} = \frac{1}{\beta} = \frac{R_1+R_f}{R_1} = 1 + \frac{R_f}{R_1}$

$\Rightarrow A_{v_f} = 1 + \frac{R_f}{R_1}$ (same as got for non-inverting op-amp)

eg Consider the circuit given below.



Suppose the amplifier suffers from offset & we have:

$I_+ = I_- = 50\,nA$

$V_{os} = -1\,mV$

$V_1 = 2\,mV$

$V_2 = 20\,mV$

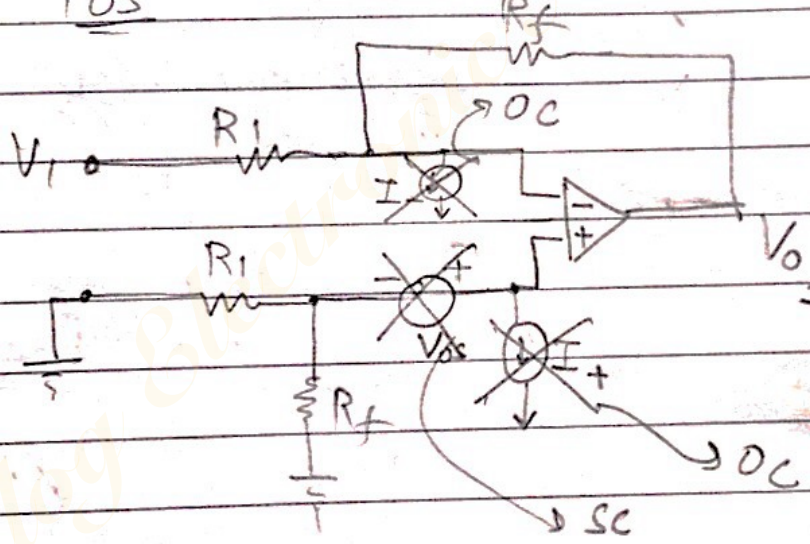
$R_f = 100K$

$R_1 = 10K$

Find: V_o

Clearly the circuit has more than one source. So, use POS

Taking only V_1



Now, $V_{o1} = -\left(\frac{R_f}{R_1}\right) V_1$

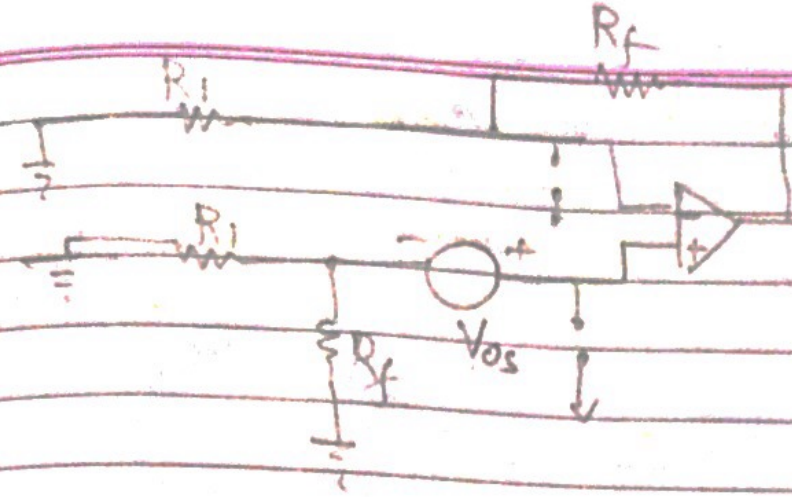
Taking only V_2

$$V_{o2} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_f}{R_1 + R_f}\right) V_2$$

V_+

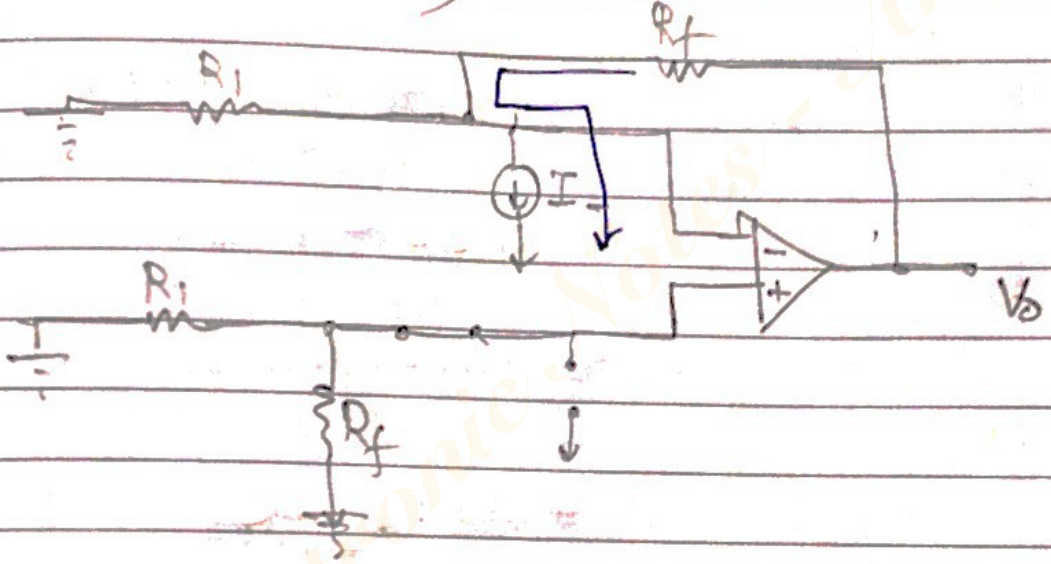
$$\Rightarrow V_{o2} = \left(\frac{R_f}{R_1}\right) V_2 .$$

Taking only V_{os}



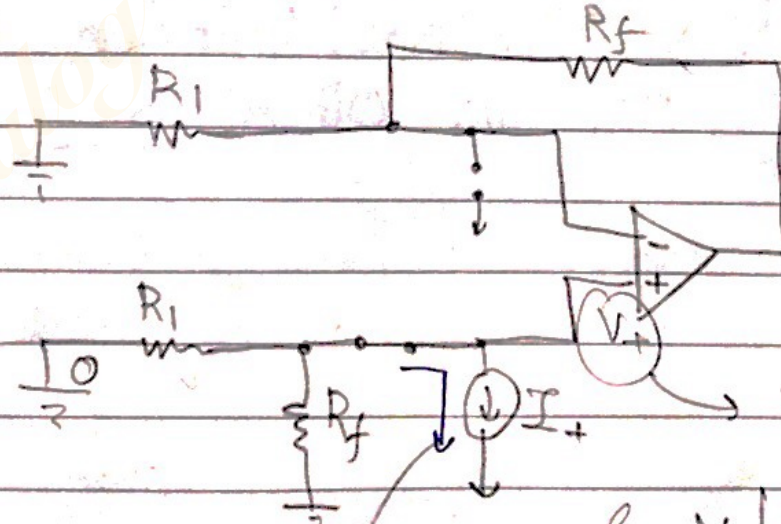
$$V_o\Big|_{V_{os}} = \left(1 + \frac{R_f}{R_1}\right) V_{os}.$$

Taking only I_-



$$-V_o\Big|_{I_-} = R_f I_-.$$

Taking only I_+



lower to higher potential

opposite direction

$$V_+ = (-I_+)(R_f \parallel R_1)$$

$$\text{So, } V_o\Big|_{I_+} = \left(1 + \frac{R_f}{R_1}\right)(V_+)$$

dir^n of current is from lower potential to higher potential. So, its (-ve)

$$\Rightarrow (V_o)\Big|_{I_+} = \left(1+\frac{R_f}{R_1}\right)\left(R_1 \| R_f\right)(-I_+)$$

$$= \left(\frac{R_1+R_f}{R_1}\right)\left(\frac{R_1 R_f}{R_1+R_f}\right)(-I_+)$$

$$\Rightarrow V_o\Big|_{I_+} = -R_f I_+$$

&

$$V_o\Big|_{total} = V_o\Big|_{V_1} + V_o\Big|_{V_2} + V_o\Big|_{V_{OS}} + V_o\Big|_{I_-} + V_o\Big|_{I_+}$$

$$\Rightarrow V_o = -\left(\frac{R_f}{R_1}\right)V_1 + \left(\frac{R_f}{R_1}\right)V_2 + \left(1+\frac{R_f}{R_1}\right)V_{OS} + R_f I_- - R_f I_+$$

$$= \frac{R_f}{R_1}(V_2 - V_1) + \left(1+\frac{R_f}{R_1}\right)V_{OS} + R_f(I_- - I_+)$$

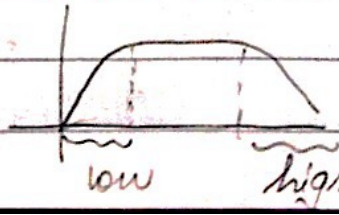
✱ FREQUENCY RESPONSE & FREQUENCY COMPENSATION IN OP-AMPS

What happens to freq. response in CE-Amps?

① low freq, $\left(X_C = \frac{1}{\omega C}\right)$ $\Rightarrow X_C$ is very high. So, capacitors blocks all DC.

② high freq; device capacitance comes into picture

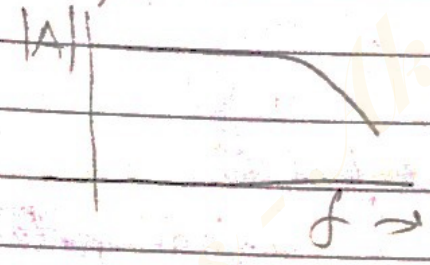
freq. response



What happens in OP-AMP?

Unlike CE Amplifiers, coupling capacitors at i/p are absent. So, it gives an excellent low freq. response.

But, at high freq, the device capacitance is still there. And, ∵ no. of poles are more, so, the high freq. response is complex.



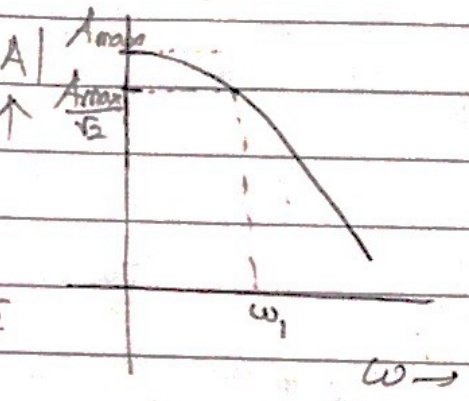
Now,

Consider a single pole.

$$A(j\omega) = \frac{A_{max}}{1 + j\left(\frac{\omega}{\omega_1}\right)}$$

→ gain at low freq

$$\hookrightarrow |A| = \frac{A_{max}}{\sqrt{1 + \left(\frac{\omega}{\omega_1}\right)^2}}$$



→ for $\omega << \omega_1$

$|A| = A_{max}$.

→ for $\omega = \omega_1$

$|A| = A_{max}/\sqrt{2}$

→ for $\omega >> \omega_1$

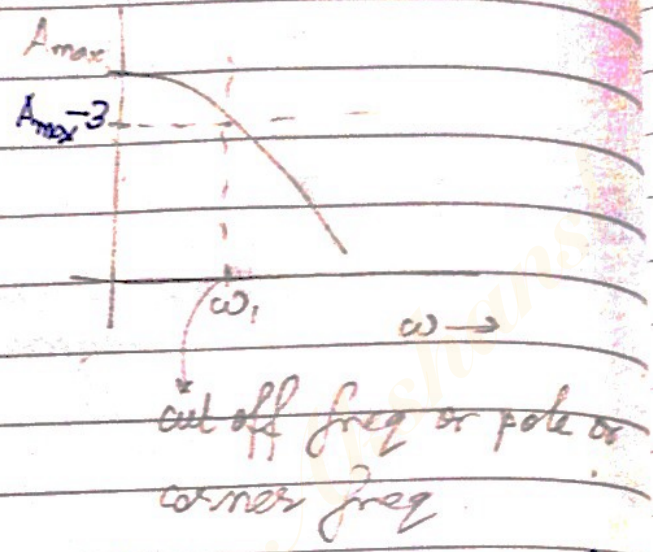
$|A| = \frac{A_{max} \times \omega_1}{\omega}$.

A_{max} can have a large value.

So, ∵ values vary, the vertical axis is plotted in log scale. So, we do ∵ 20 log|A|. Hence, we take dB values.

So, $|A|_{dB} = 20 \log(|A|)$

So, scale becomes

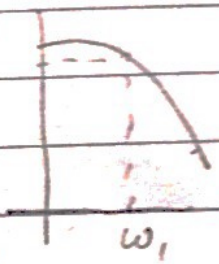


~~cut off freq or pole or~~ corner freq

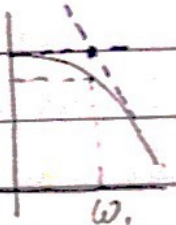
* Bode Plot:

A linearity of actual plot that you'll get when you plot gain (dB) vs frequency (rad/sec)

Idea: our actual graph was:



If we plot in log scale



It will always be such that the intersection of the tangents will always be the same line for ω_1.

So, ω_1 is called Pole or Corner Point.

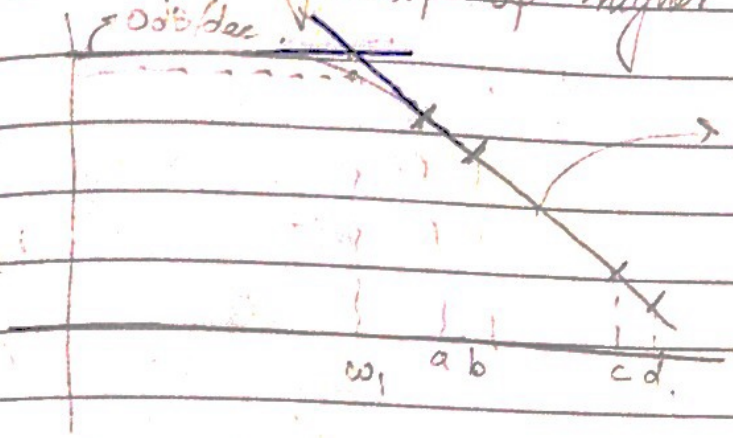
Hence, idea of Bode plot is used so we get the same pole.

Q What is 0 dB/dec

Decade means how much span is done on the graph. i.e, going from 1 to 10 or 10 to 100 or 100 to 1000 ....

Now, 0 dB/dec means that the gain remains 0 dB throughout one decade.

Now, seeing slope of higher freq. part



Now, we plot bode plot to see or study the poles.

We know that bode plot is an approxim^n. we do (∵ we take tangents to curves)

Now for finding slope, if we take b/w a & b, we are finding slope in the region which is itself an approxim^n.

So, we find slope at pts faraway from ω_1. So, choose pts. c & d.

Now,

eq^n of gain, $|A| = \dfrac{A_{mav}}{1+\left(\frac{\omega}{\omega_1}\right)^2}$.

↳ for $\omega >> \omega_1$, $|A| = \dfrac{A_{mav}\,\omega_1}{\omega}$

So, for high freq part, $|A| = A_{mav} \times \dfrac{\omega_1}{\omega}$.

↳ for $\omega|_{pt.c} = 100\omega_1$, say.

$\Rightarrow |A| = \dfrac{A_{mav}}{100}$ → (1)

$|A|_{dB} = 20\log\dfrac{A_{mav}}{100} = 20\log(A_{mav}) - 40$. → (1)

↳ one decade later;

$\omega|_{pt\ d} = 1000\ \omega_c$

$\Rightarrow |A| = \frac{A_{max}}{1000}$

& $|A|_{dB} = 20\log\left(\frac{A_{max}}{1000}\right)$

$\Rightarrow |A|_{dB} = 20\log(A_{max}) - 60$ ——— (2)

From (1) & (2),

$(A)_{pt.d} - (A)_{pt\,c}$

$= \left(20\log(A_{max}) - 68\right) - \left(20\log(A_{max}) - 40\right)$

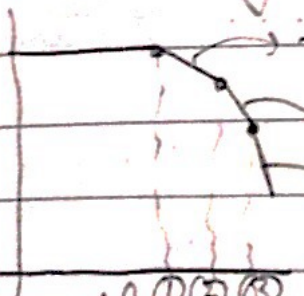
$\Rightarrow$ Slope $= -20$

$\Rightarrow$ So, Slope $= -20$ dB/dec for high freq

✡ Open loop gain, A of OP-AMP

Note :- If the no. of poles increase, the slope keeps on decreasing

eg :- for 3 poles.



It is visible that the slope is decreasing everytime

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Q What is Octave?

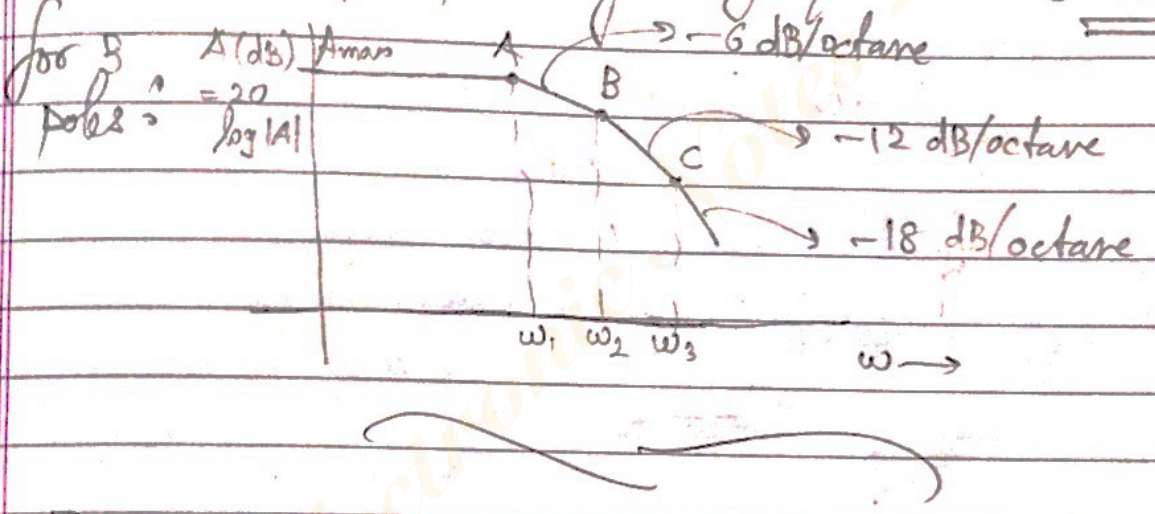
In this the span of frequency is TWO

i.e, ω_1 ——— ω_2 . Then, $\omega_2 = 2\omega_1$.

(like in decade

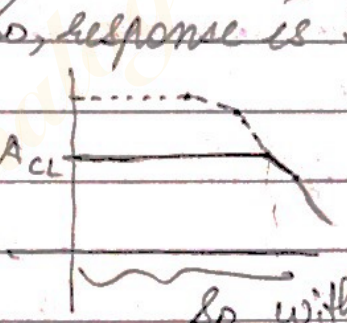
ω_1 ——— ω_2 , $\omega_2 = 10\omega_1$)

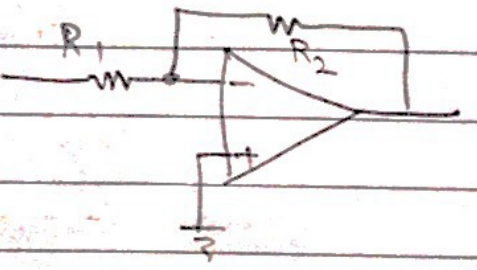
Why it can be seen that in octave scale the slope for higher freq is −6 dB/dec.



* For a closed loop circuit, $\left|A_{CL}\right| = \left(\frac{R_2}{R_1}\right)$

So, response is :-





So, with CL, our OP-amp can operate at wider freq. range

Why this reduction? → In CL, ∃ feedback. So, gain is stabilised but has a lower value. However, ∃ decrease in gain at higher frequencies.

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* Consider an op-amp w.r.t of gain is high until frequency reaches ω_2 as shown

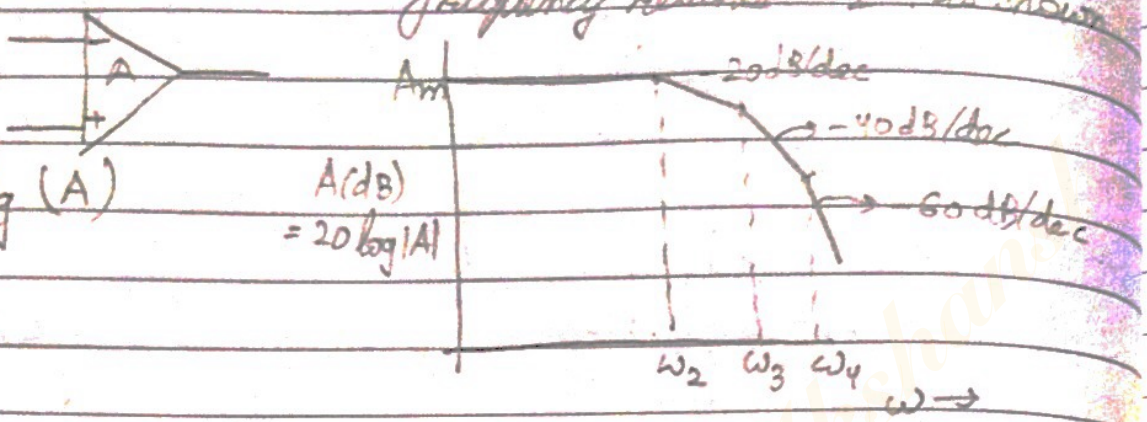


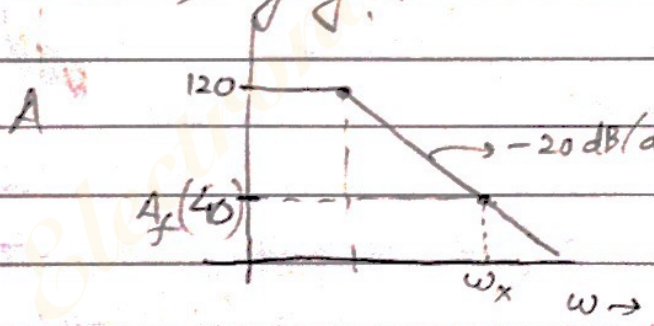
fig (A)

So, ∃ 3 poles.

If the op-amp in fig (A) follows the above characteristic, then, using this op-amp for any applicⁿ will show fluctuation at high frequency. So, ∃ defects in the form of poles.

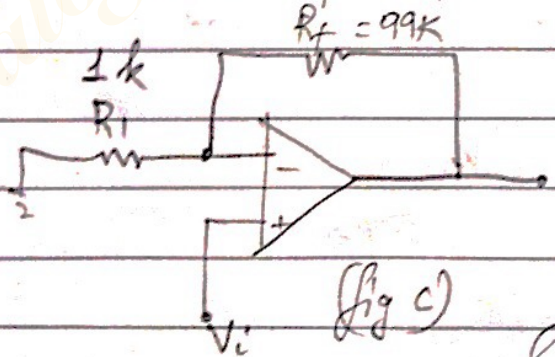
We have to correct these defects.

(like, trying to make one pole, instead of 3)



(fig B)

Consider an op-amp satisfying above char.



(fig c)

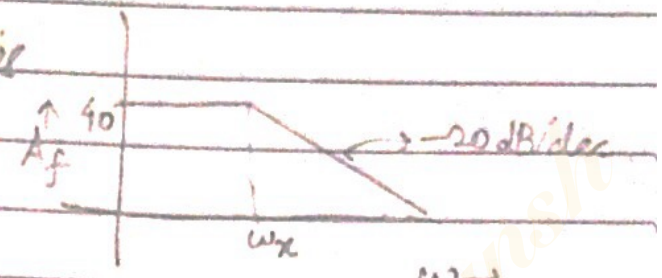
$$A_f = \left(1 + \frac{R_f}{R_1}\right) = 100.$$

$$A_f\big|_{dB} = 40\ dB.$$

So, the gain of amplifier should give gain of 40 dB.

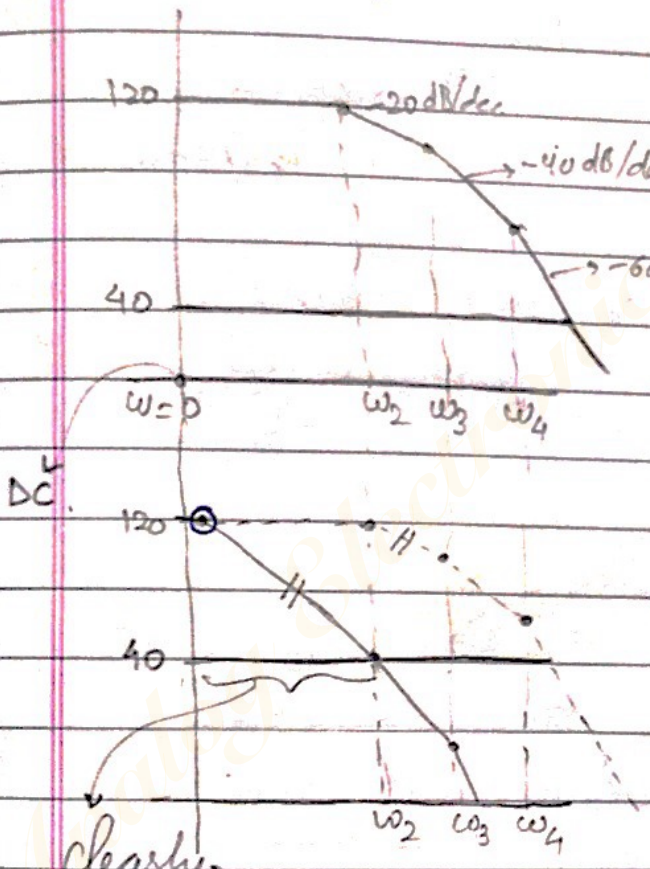
From fig (B), if $\omega > \omega_x$, A_f falls below 40dB

So, CL gain for fig (C) is



∴ no instability in this feedback amplifier. So, CL response is good (stable) & can be used

How to compensate instabilities ?



Suppose I add an additional pole at lower freq. So, from that point itself, I a fall of -20dB/dec

Clearly, this region experiences only one pole. So, sys. is much more stable now.

Method 1:
Called as Dominant Pole Compensation
(PTO for details)

$A\beta$: Loop gain.

$|A\beta|_{dB} = 20 \log(A\beta)$

Note : OL gain $= \frac{A}{1+A\beta} = \frac{1}{1/A + \beta}$

If $A >> 1$

$\Rightarrow$ OL gain $\simeq \frac{1}{\beta}$

$|A\beta|_{dB} = 20 \log(A\beta)$

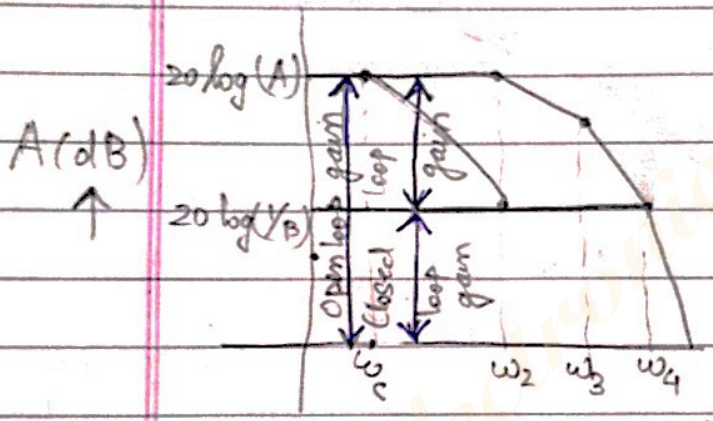
$= 20 \log A - 20 \log\left(\frac{1}{\beta}\right)$

For us, say $A >> 1 \Rightarrow$ Gain $= \frac{1}{\beta}$

$\Rightarrow 20 \log\left(\frac{1}{\beta}\right) = 40$ dB

in our problem.

(Closed loop gain)



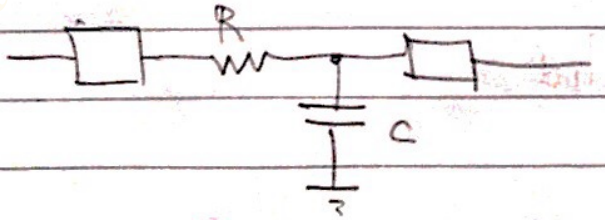
OL gain $= 20 \log(A)$

CL gain $= 20 \log\left(\frac{1}{\beta}\right)$

$\omega \rightarrow$ loop gain $= 20 \log(A\beta)$

Note : As freq. $\uparrow$, loop gain $\downarrow$.

Dominant pole compensation.



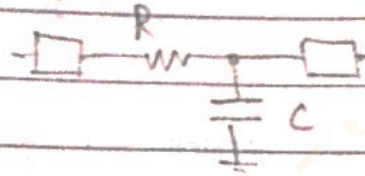
$\omega_c = \frac{1}{R_{eq} C}$.

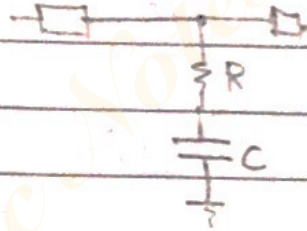
i.e., we put an RC circuit s.t its freq. is close to freq. of zero.

The idea is to put a pole at such freq at the decrease in slope that it causes, remains constant until 2nd pole (at ω_2) comes.

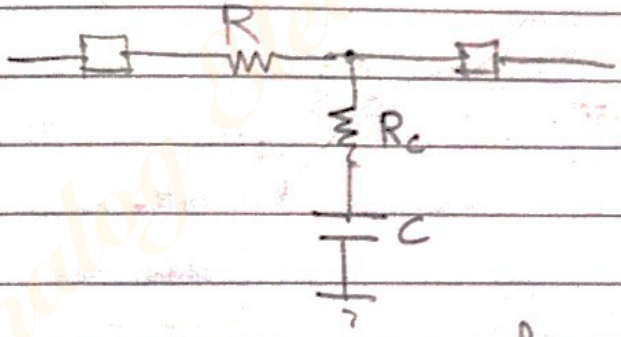
Pole zero compensation.

Idea: Pole causes decrease in slope
Zero causes increase in slope

So, if we put  we get pole.

&  we get zero.

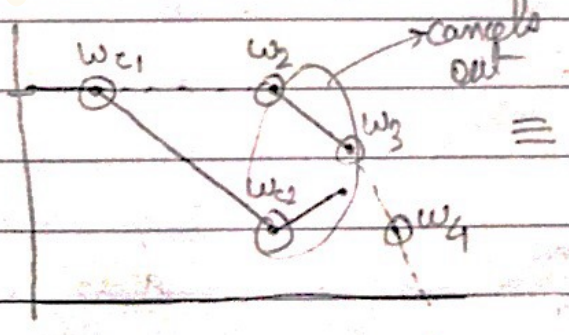
If both poles & zeros are added, net = constant
So, additional circuit to be added:



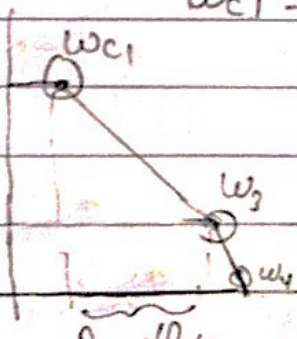
The diff is in the value of freq. of pole & zero

$\omega_{c2} = 1/RC$

$\omega_{c1} = 1/(R+R_c)C$



≡



In this BW, gain is stable & constant.

Consider the idea:

Poles at $\omega_{c1}, \omega_2, \omega_3, \omega_4$

Zero at ω_{c2}

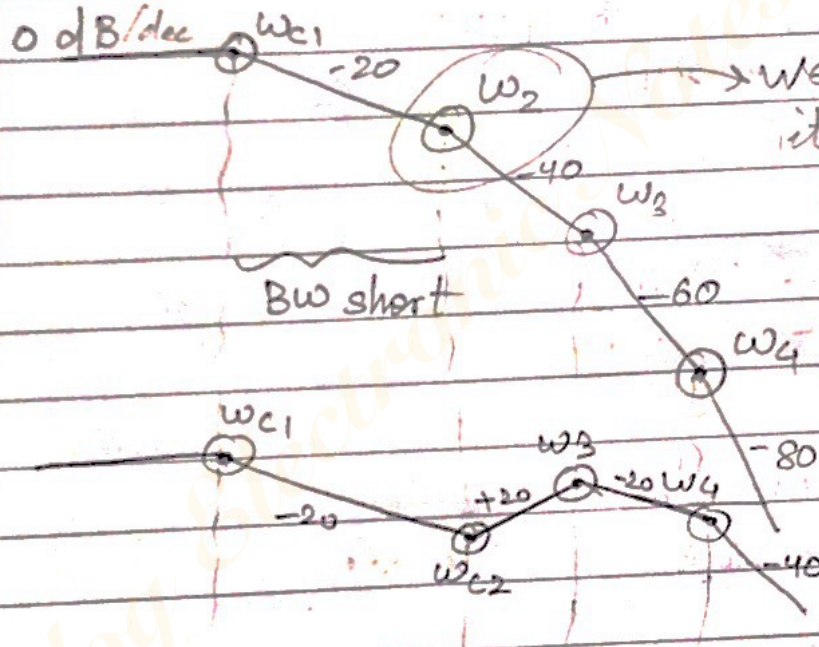
So, gain =

$$A = \frac{A_m\left(1+j\frac{\omega}{\omega_{c2}}\right)}{\left(1+j\frac{\omega}{\omega_{c1}}\right)\left(1+j\frac{\omega}{\omega_2}\right)\left(1+j\frac{\omega}{\omega_3}\right)\left(1+j\frac{\omega}{\omega_4}\right)}$$

Now, we want to increase the BW

Once ω_{c1} comes, ∃ a ↓ in gain with slope of −20 dB/dec. When ω_{c2} comes ∃ ↑ in slope to 0 dB/dec. When ω_2 comes ↓ to −20 dB/dec.

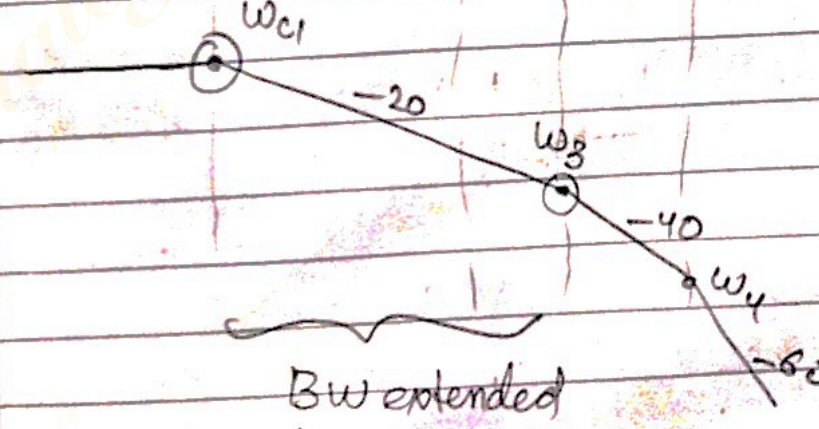
fig ①



→ we want to remove it s.t. our slope remains −20 dB/dec. So, put a zero, exactly at ω_2 ($\omega_2 = \omega_{c2}$)

fig ②

fig ③ = fig ① + fig ②



As shown in the fig. (Also, from the formula, if $\omega_2 = \omega_{c2}$ the terms in numerator & denominator cancels out)

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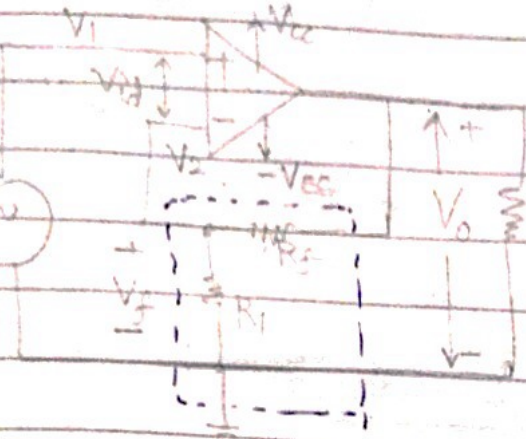
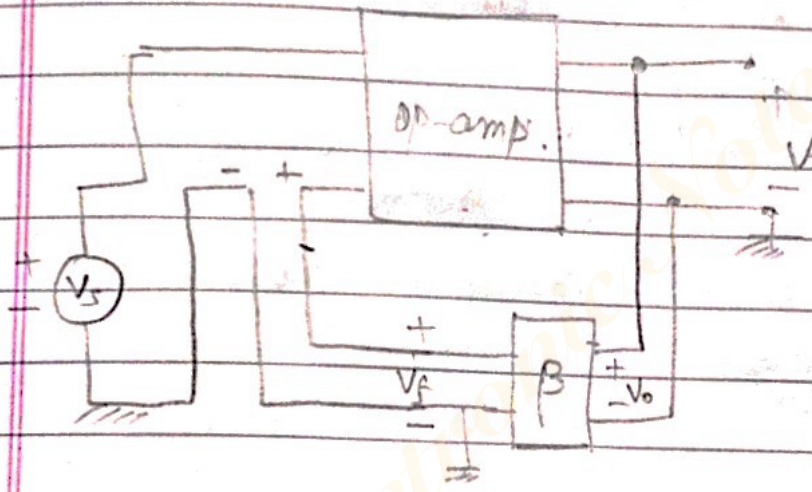
✱ Consider a non-Inverting op-amp.



Idea: we want to see the circuit in the form of A & β so as to get A_f

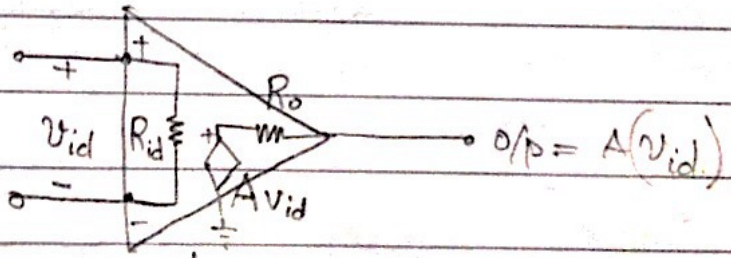
$$A_f = \frac{A}{1+A\beta}$$

fig (1)



Shunt - series

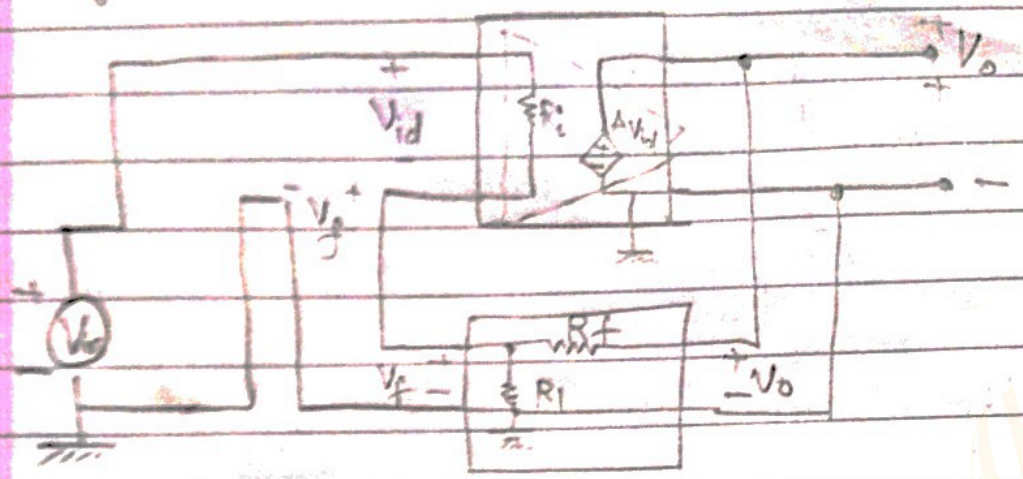
Assume op-amp has OL gain = A (ideally $\to \infty$)
Seeing equivalent model of op amp :
(Non-ideal)



↳ Its a voltage controlled voltage source

Use this in fig (1) alongwith the circuit

Fig (1) with β & A identified :-



$$\therefore V_o = A(V_{id})$$
$$= A(V_{in} - V_f)$$
$$= A\left(V_{in} - \left(\frac{R_1}{R_1+R_f}\right)V_o\right)$$
$$= AV_{in} - \left(\frac{AR_1}{R_1+R_f}\right)V_o$$
$$\Rightarrow V_o\left[1 + \frac{A}{1+\left(\frac{R_f}{R_1}\right)}\right] = AV_{in}$$
$$\Rightarrow \frac{V_o}{V_{in}} = \left(\frac{A}{1+\frac{A}{1+\left(\frac{R_f}{R_1}\right)}}\right)$$

↳ If $\frac{R_1}{R_1+R_f} = \frac{1}{1+\left(\frac{R_f}{R_1}\right)} = \beta$

(voltage divider b/w R_f & R_1)

$$\Rightarrow \frac{V_o}{V_{in}} = \boxed{A_f = \frac{A}{1+A\beta}}$$

↳ feedback gain.

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Using i/p resistance of amplifier with feedback.

If i/p mixing is in series then i/p resistance ↑ by a factor of $(1+A\beta)$.

resistance ↑

$= \frac{V_{in}}{I_{in}} = \frac{V_{in}}{V_i/R_i}$

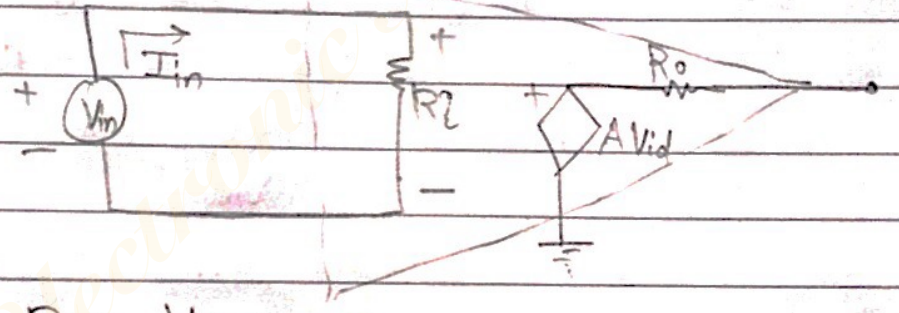
$$R_{if} = R_i(1+A\beta)$$

If sampling was shunt, o/p resistance ↓ by a factor of $1/(1+A\beta)$.

resistance ↓

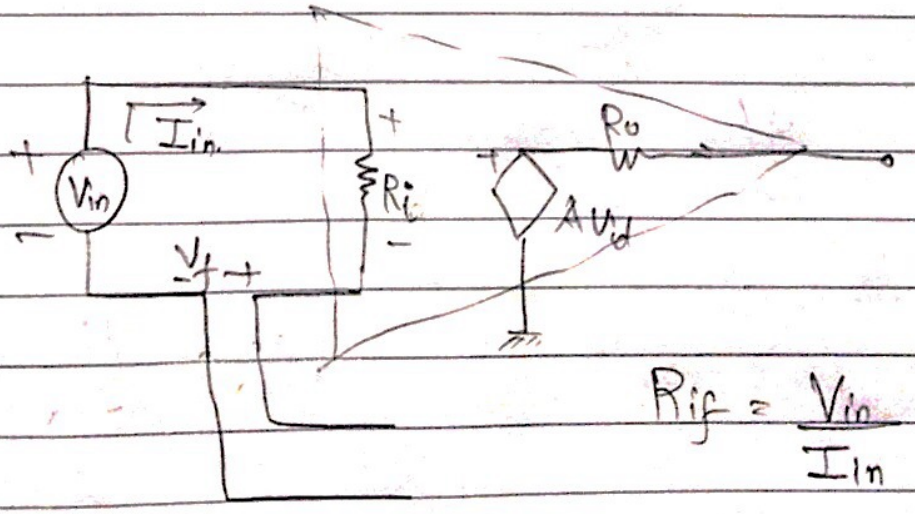
$$R_{of} = \frac{R_o}{1+A\beta}.$$

op-amp before feedback



$$R_i = \frac{V_{in}}{I_{in}}.$$

op amp after feedback



$$R_{if} = \frac{V_{in}}{I_{in}}$$

$$R_{if} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{V_{id}/R_i}$$

(Note: before, $V_{in} = V_{id}$
after fb, $V_{in} \neq V_{id}$)

$$V_{id} = \frac{V_o}{A} \quad (\because V_o = A V_{id})$$

Also, $V_o = A_f V_{in}$ (from feedback)

& $A_f = \frac{V_o}{V_{in}}$.

$$\Rightarrow V_o = \frac{A}{1+A\beta} V_{in} \quad \left(\because A_f = \frac{A}{1+A\beta}\right)$$

$$V_{id} = \frac{V_o}{A} = \frac{V_{in}}{1+A\beta}$$

$$\therefore R_{if} = \frac{V_{in}}{V_{id}} \times R_i$$

$$= \frac{V_{in}}{V_{in}/1+A\beta} \times R_i$$

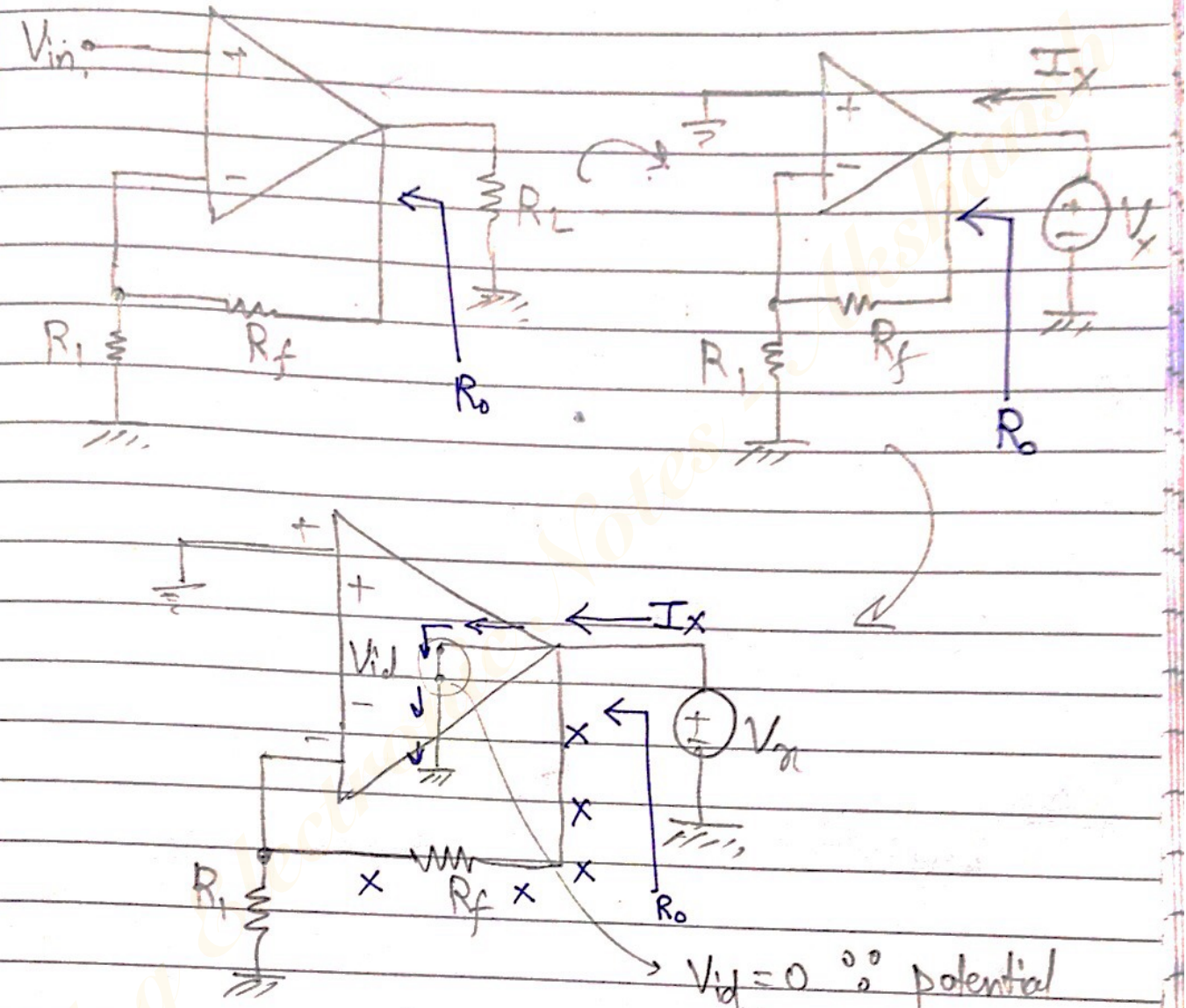
$$\Rightarrow R_{if} = (1+A\beta) R_i$$

✓

Q. Consider a circuit. Find its op resistance (R_o)

Idea: Replace R_L by voltage source (V_x) & current I_x. Then, short all DC voltage sources. Now,

$$R_o = \frac{V_x}{I_x}$$



$V_{id} = 0$ ∴ potential

$V_+ = V_- = 0$.

I_x flows inside (towards $R=0$ side instead of R_f).

So, $R_o = 0$

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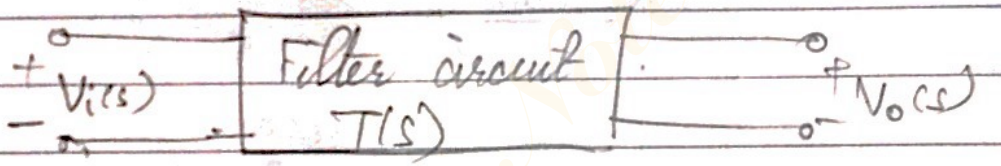
ACTIVE FILTERS

↳ a circuit that is capable of removing some freq. from i/p & leaving remaining freq's.

* Use of active filter :
It amplifies as well as filters.

* Function :
to stop some band and pass some band.



$$TF = T(s) = \text{Gain} = \frac{V_o(s)}{V_i(s)}$$

→ $s = \sigma + j\omega$.

→ for physical freq's

freq of source that we are setting

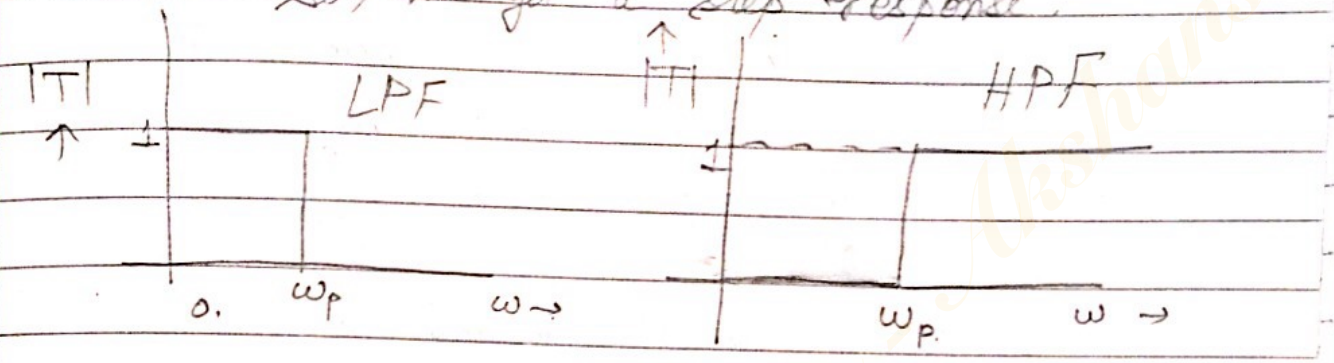
$$T(j\omega) = |T(j\omega)|\, e^{j\phi(\omega)}$$

→ both gns of freq.

Why do we see TF of a filter ?
We see freq response.

• Ideal transmission char.

↳ Filter passes (all) the freq in some range & doesn't pass at all in some range - So, we get a step response.

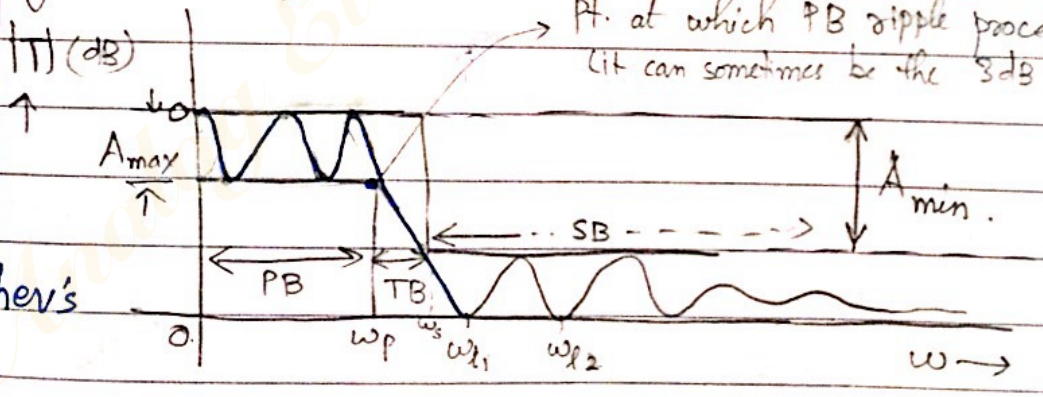


Hy BPF & BSF ....

* Filter Design :

↳ done by using PRACTICAL Transmission char. (no abrupt change)

Consider practical transmission char. of Low pass filter (LPF)



Chebyshev's Filter

(fig 1)

PB = Pass band

TB = Trans^n band

SB = Stop band.

Objective: 1) Design TF with
2) Reduce order & BSB (monotonically decreasing)

So, parameters that specify design:

1. A_{max} : Should be small
2. A_{min} : Should be large
3. PB edge ω_p : } ω_p, ω_s close to each other
4. SB edge ω_s : }

Transfer fn, general form:

$$TF = T(s) = \frac{a_M s^M + a_{M-1} s^{M-1} + \cdots + a_1 s + a_0}{s^N + b_{N-1} s^{N-1} + \cdots + b_1 s + b_0}$$

→ Order of s in numerator < Order of s in den.

i.e. $M < N$

→ $s = \sigma + j\omega$.

Ok,

$$T(s) = a^M \frac{\prod_{m=1}^{M} (s - Z_m)}{\prod_{n=1}^{N} (s - P_n)}$$

→ $Z_1, Z_2, \cdots Z_m$ the zeroes.

→ $P_1, P_2, \cdots P_n$ the poles

→ expressing it as a factor of poles & zeroes

(like $\frac{x^2+2x+1}{x^2-3x+2} = \frac{(x+1)(x+1)}{(x-1)(x-2)}$

→ Zeroes = $-1, -1$

→ Poles = $1, 2$.)

* All complex poles/zeros always occur in conjugate pairs.

Now, $s = \sigma + j\omega$.

⇒ Poles & zeros can be real / imaginary

From fig ①, we find, zero's (pts. where magnitude = 0) occur on ($j\omega$) axis

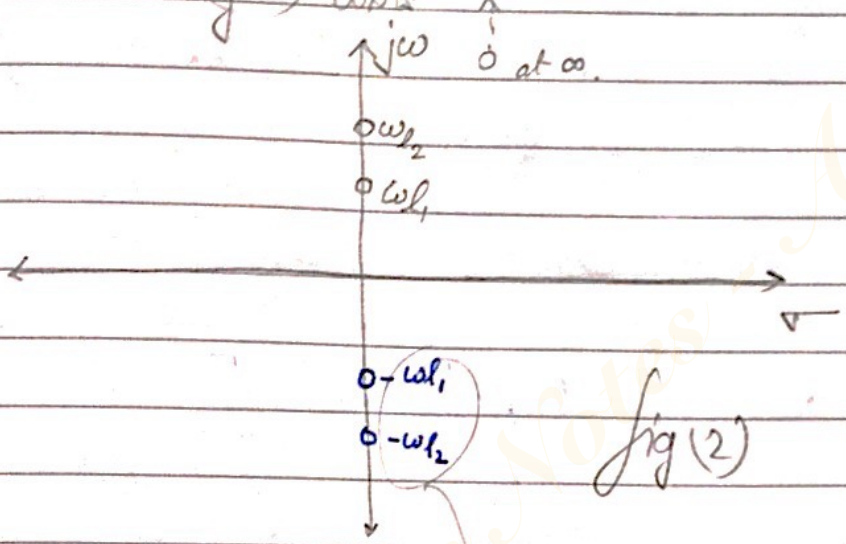


fig (2)

complex conjugate to the zero's $j\omega_{l_1}$ & $j\omega_{l_2}$

So, ∃ 5 zeros.

Hence, numerator poly. is given as:- (not considering at ∞)

$$= (s - j\omega_{l_1})(s + j\omega_{l_1})(s - j\omega_{l_2})(s + j\omega_{l_2})$$

$$= (s^2 + \omega_{l_1}^2)(s^2 + \omega_{l_2}^2) = (-\omega^2 + \omega_{l_1}^2)(-\omega^2 + \omega_{l_2}^2)$$

From fig ①, seeing poles.

→ For $s = j\omega$ (in terms of physical frequency)
→ O/P = TF = 0.
if $\omega = \omega_{l_1} = \omega_{l_2}$

No. of zeros = 5. So, poles can be 5 or more. For simplicity, take 5.

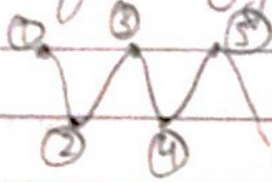
⇒ Denominator poly:

$$s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0$$

Till now we have got

$$TF = \frac{a_4 (s^2 + \omega_{z_1}^2)(s^2 + \omega_{z_2}^2)}{s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

So, from fig ① also, the PB side is



: Demarkates that ∃ 5 poles.

Now, for 5 poles ⇒ (5 real)
or (2 complex conjugate pairs + 1 real)

So, poles can be

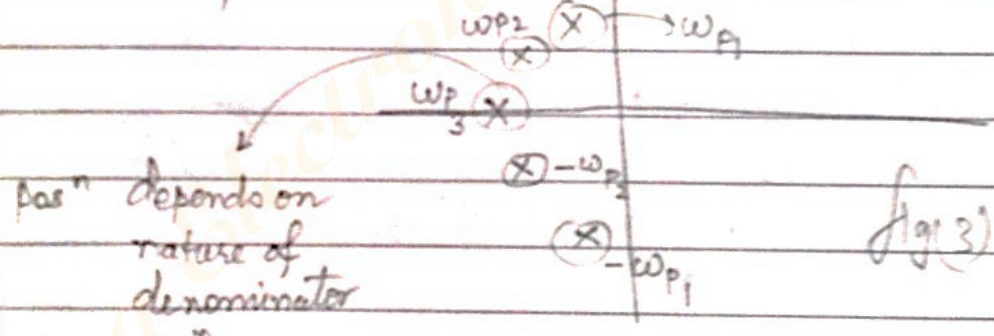


Fig (3)

pos^n depends on nature of denominator eq^n

* Note :- ✓ Stable networks have poles on left of imaginary axis.
✓ poles on imaginary axis indicates undamped sinusoidal o/p
✓ Poles on -ve real axis indicates damped exponential response.

Seen in Butterworth ⇒ If we see the bode plot, every pole reduces response with slope (−20 dB/dec). Now, if we can make all poles to come at one freq, response comes down, rolls off, fast as ideal.

From fig (1)

↳ we note value of A_{max}, A_{min}, ω_1 & ω_2 to make any filter's freq. response

Now, finding denominator polynomial of order (5) or more.

consider 5 poles

☆ Note:

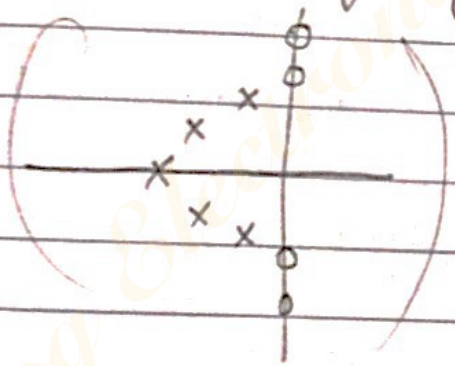
Any pole on jω axis ⇒ sustained oscill^n

Any pole on real axis ⇒ exponential decay

So, our 5 poles = 2 complex conjugates + 1 real pole

So,

our final model for fig(1) = fig(2) + fig(3)

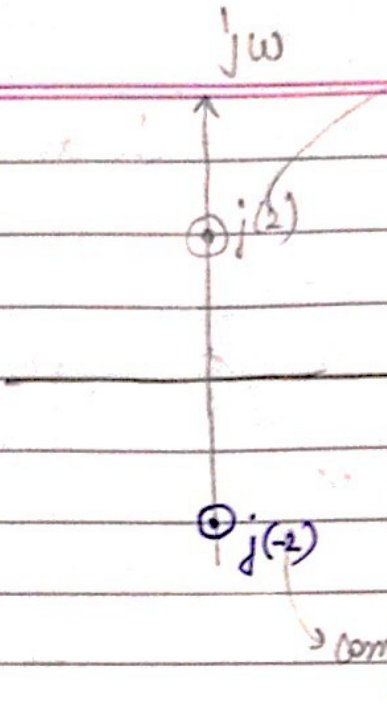


eg. A 2nd order filter has 2 poles at $\frac{-1}{2} \pm j\frac{\sqrt{3}}{2}$.

∃ transmission zero at $\omega = 2$ rad/s & unity at $\omega = 0$.

Find TF

Idea: Draw jω axis & σ axis & plot cond^n



For numerator poly:

$(s-z_1)(s-z_2)$

$z_1 = j2$

$z_2 = -j2$

$= (s-j2)(s+j2)$

$= (s^2+4)$

So, $TF = \frac{num}{den} = \frac{s^2+4}{(\quad)}$

Denominator poly: $(s-p_1)(s-p_2)$

$p_1 = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$

$p_2 = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$

$\therefore$

$= \left(s+\frac{1}{2}-j\frac{\sqrt{3}}{2}\right)\left(s+\frac{1}{2}-j\frac{\sqrt{3}}{2}\right)$

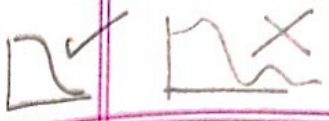
$= \left(\left(s+\frac{1}{2}\right)-j\frac{\sqrt{3}}{2}\right)\left(\left(s+\frac{1}{2}\right)+j\frac{\sqrt{3}}{2}\right)$

$\Rightarrow$ Den. poly. $= \left(s+\frac{1}{2}\right)^2 + \frac{3}{4}$

So, $TF = \frac{s^2+4}{(s+1/2)^2+3/4} = \left(\frac{s^2+4}{s^2+s+1}\right)(k)$

always keep this factor as the TF need not be normalised

✱ Monotonically decreasing ⇒ continuously decreasing.
∃ no question of coming up.



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Now, we know, Transmission = 1 at $\omega = 0$

$$\Rightarrow T(0) = \frac{k(0+4)}{(0+0+1)}$$

$$\Rightarrow 4k = 1$$

$$\Rightarrow k = 1/4$$

$$\Rightarrow TF = \left(\frac{1}{4}\right)\left(\frac{s^2+4}{s^2+s+1}\right)$$ Ans

✱ MAXIMALLY FLAT RESPONSE - Butterworth Filters.

∴ we define ω_c (cut off freq) so, we are close to ideal Pass band area. So, that part (at ideal) is flat

✱ Note: We want monotonically decreasing graph. So, there should NEVER be finite zeros (∵ with finite zero, it'll come to 0, then go up)

So, TF = $\frac{k}{(\quad)+(\quad)\ldots}$

So, $$H(s) = \frac{K}{s^N + b_{N-1}s^{N-1} + \ldots + b_1 s + b_0}$$

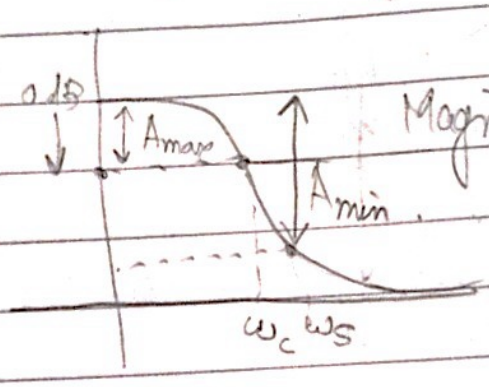
In some special case, I can express $\frac{s^N + b_{N-1}s^{N-1} + \ldots + b_0}{\text{into } \sqrt{1+\epsilon^2\left(\frac{\omega}{\omega_c}\right)^2}}$

↳ Normalized maximally flat response:

$$|H(j\omega)| = \sqrt{\frac{1}{1+\epsilon^2\left(\frac{\omega}{\omega_c}\right)^{2N}}}$$

At corner freq $\Rightarrow \omega = \omega_c$

$\Rightarrow |H(j\omega)| = \text{Magnitude} = \frac{1}{\sqrt{1+\epsilon^2}} = |A|_{max}$



$$\text{Magnitude}_{dB} = 20\log\left[\frac{1}{\sqrt{1+\epsilon^2}}\right] = -20\log\sqrt{(1+\epsilon^2)}$$

↳ ϵ : Max. deviation in PB.

$$\epsilon = \sqrt{10^{(A_{max}/10)} - 1}$$

At edge of SB, $\omega = \omega_s$

$$A(\omega_s) = 20\log\frac{1}{\sqrt{1+\epsilon^2\left(\frac{\omega_s}{\omega_c}\right)^{2N}}}$$

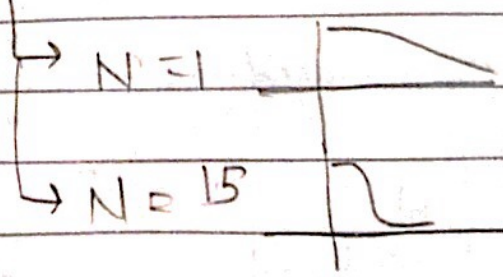
$$\Rightarrow A(\omega_s) = -10\log\left[1+\epsilon^2\left(\frac{\omega_s}{\omega_c}\right)^{2N}\right]$$

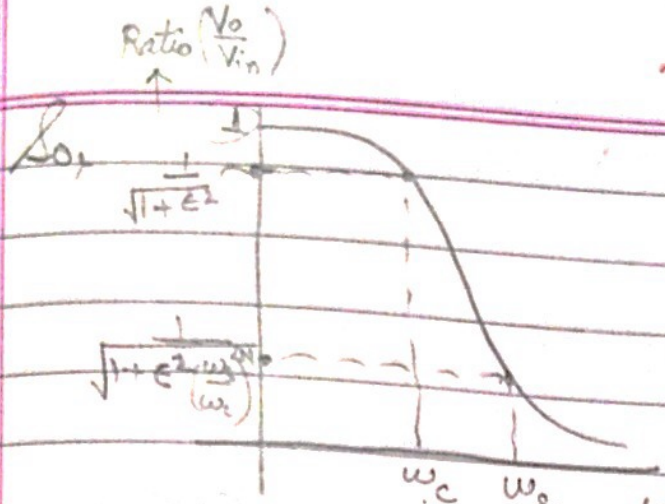
Now, seeing for ω_s is close to ω_c.

$$\Rightarrow |A(\omega_s)| = 10\log\left[1+\epsilon^2\left(\frac{\omega_s}{\omega_c}\right)^{2N}\right]$$

↳ N = 1

↳ N = 15





For dB

At ω_c : $|A_{max}| = -20 \log \sqrt{1+\epsilon^2}$

At ω_s : $|A_{min}| = -10 \log \left[1+\epsilon^2\left(\frac{\omega_s}{\omega_c}\right)^{2N}\right]$

* Lower order → less ideality.

* Value of ϵ : can vary on design.

eg: Design a filter:

$\omega_c = 1$, $\epsilon = 1$, given.

$$\Rightarrow |H(j\omega)| = \frac{1}{\sqrt{1+\epsilon^2\left(\frac{\omega}{\omega_c}\right)^{2N}}}$$

$$|H(j\omega)| = \frac{1}{\sqrt{1+(\omega)^{2N}}} \Rightarrow |H(j\omega)|^2 = \frac{1}{1+(\omega)^{2N}}$$

$$\Rightarrow H(s)H(-s) = \frac{1}{1+\omega^{2N}} = \frac{1}{1+(s/j)^{2N}}$$

$\because a \cdot a^* = |a|^2$

Finding poles:-

$$1+(s/j)^{2N} = 0$$

$$\Rightarrow (-1)^{-N} s^{2N} + 1 = 0.$$

Case (1):- N = even

$$\Rightarrow s^{2N} = -1 = e^{j(2k-1)\pi}$$

So, $\exists$ 2N roots for s

$$p_k = \exp\left(j\frac{2k-1}{2N}\pi\right) = \exp(j\theta_k)$$

$\rightarrow k = 1, 2, \ldots, 2N$

Case (2) :- N = odd,

$$s^{2N} = 1 = e^{j(2k)\pi}$$

Here also, $\exists$ $2N$ roots for s :-

$$p_k = \exp\left(j\frac{k}{N}\pi\right) = \exp(j\theta)$$

$\rightarrow k = 0, 1, 2, \ldots (2N-1)$

So,

$$TF\Big|_{N=\text{even}} = |H(s)| = \frac{1}{\prod_{K=1}^{N/2}\left(s^2 + 2s\cos\theta_K + 1\right)}$$

$\rightarrow \theta_k = \left(\frac{2k-1}{2N}\right)\pi$

&

$$TF\Big|_{N=\text{odd}} = H(s) = \frac{1}{(s+1)\prod_{K=1}^{(N-1)/2}\left(s^2 + 2s\cos\theta_K + 1\right)}$$

$\rightarrow \theta_k = \left(\frac{k}{N}\right)\pi$

1st order filter,
3rd order filter ....

$\rightarrow$ Note : We had

$$H(s).H(-s) = \frac{1}{1 + \left(\frac{s}{jf}\right)^{2N}}$$

So, $|H(s)|^2$ has a polynomial of order $2N$

So, $H(s)$ has an order of N

eg :- If N = 1 given. Find TF

⇒ 1st order filter :-

⇒ Use $H(s) = \frac{1}{(s+1)\prod_{K=1}^{(N-1)/2}(s^2 + 2s\cos\theta_K + 1)}$

⇒ $H(s) = \frac{1}{s+1}$ ✓

If N = 2

⇒ 2nd order filter :-

$H(s) = \frac{1}{\prod_{K=1}^{1}(s^2 + 2s\cos\theta_K + 1)}$

$= \frac{1}{s^2 + 2s\cos\theta + 1}$

↳ $\theta = \pi/4$.

⇒ $H(s) = \frac{1}{s^2 + \sqrt{2}s + 1}$

If N = 3

$H(s) = \frac{1}{(s+1)(s^2+s+1)}$

* If we design for any other ω_c ($\omega_c \neq 1$) simply replace $s \longrightarrow \frac{s}{\omega_c}$ in every formula (Thumb rule for solving)

eg : $H(s) = \frac{1}{s+1}$; $\omega_c = 1$, N = 1

then, $H(s) = \frac{1}{(s/10)+1}$; $\omega_c = 10$, N = 1

Normally we'll take $\epsilon = 1$

- For case with $\epsilon \neq 1$, P_K will be multiplied with $\epsilon^{1/N}$.

So, for $\omega_c \neq 1$, $N = 2$

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \rightarrow \frac{1}{\sqrt{\left(\frac{s}{\omega_c}\right)^2 + \sqrt{2}\left(\frac{s}{\omega_c}\right) + 1}}$$

$$H(s) = \frac{\omega_c^2}{s^2 + \sqrt{2}\omega_c s + \omega_c^2}$$

$$H(s) = \frac{\omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \rightarrow (1)$$

$Q = \frac{1}{\sqrt{2}}$ → for Butterworth

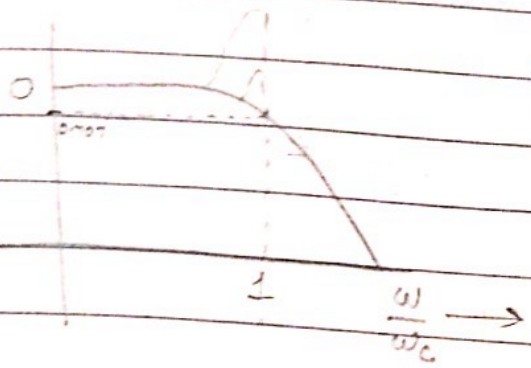
Q = Quality factor of poles

eqn (1) is quadratic in s.
So, soln:

$$P_1, P_2 = \frac{-\omega_c}{2Q} \pm j\omega_c\sqrt{1 - \frac{1}{4Q^2}}$$

↳ $Q > 0.5$ => complex roots.

- Varying ω_c changes pole distance from origin.
- Decreasing Q makes poles come closer & vice versa along semicircle.
- When $Q = 0.5$, poles meet at -ve real axis.



explained later

Filter type	Q
Butterworth	0.707
Chebyshevs	> 0.707
Bessel's	< 0.707

✱ FILTER TRANSFORMATION TECHNIQUE

Converting from LP to — Substitute s (in H(s)) to

HP	ω_c/s
BP	$[s^2 + \omega_H\omega_L]/[s(\omega_H - \omega_L)]$
BS	$s(\omega_H - \omega_L)/[s^2 + \omega_H\omega_L]$

↳ Idea : HP filter is opposite of LP filter.

So, $s \rightsquigarrow \frac{1}{s}$ or $\frac{s}{\omega_c} \rightsquigarrow \frac{\omega_c}{s}$.

Ily, BS is opposite of BP filter

$s \rightsquigarrow \underbrace{\left(\frac{s + \omega_H\omega_L}{s(\omega_H - \omega_L)}\right)}_{\text{"k, say}}$ So, for BS

$s \rightsquigarrow 1/k$

RC circuit here ⇒ V_{in} — R — V_A, C

$V_A = \left(\frac{X_c}{R + X_c}\right) V_{in}$ (Potential divider) → $X_c = 1/j\omega C$ ⇒ $V_A = \frac{V_{in}}{1 + j2\pi fRC}$

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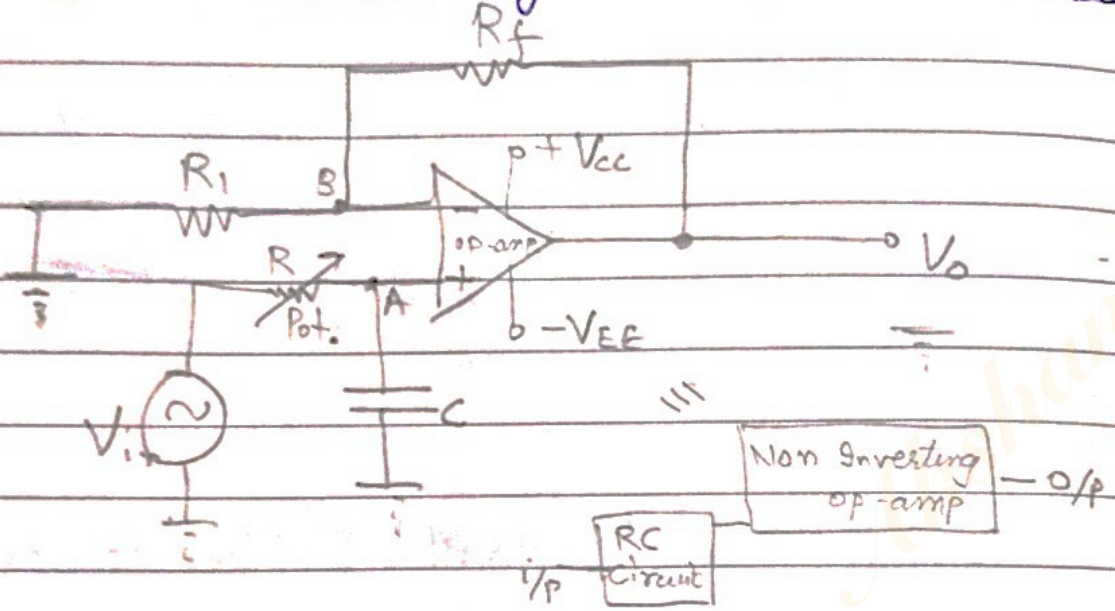
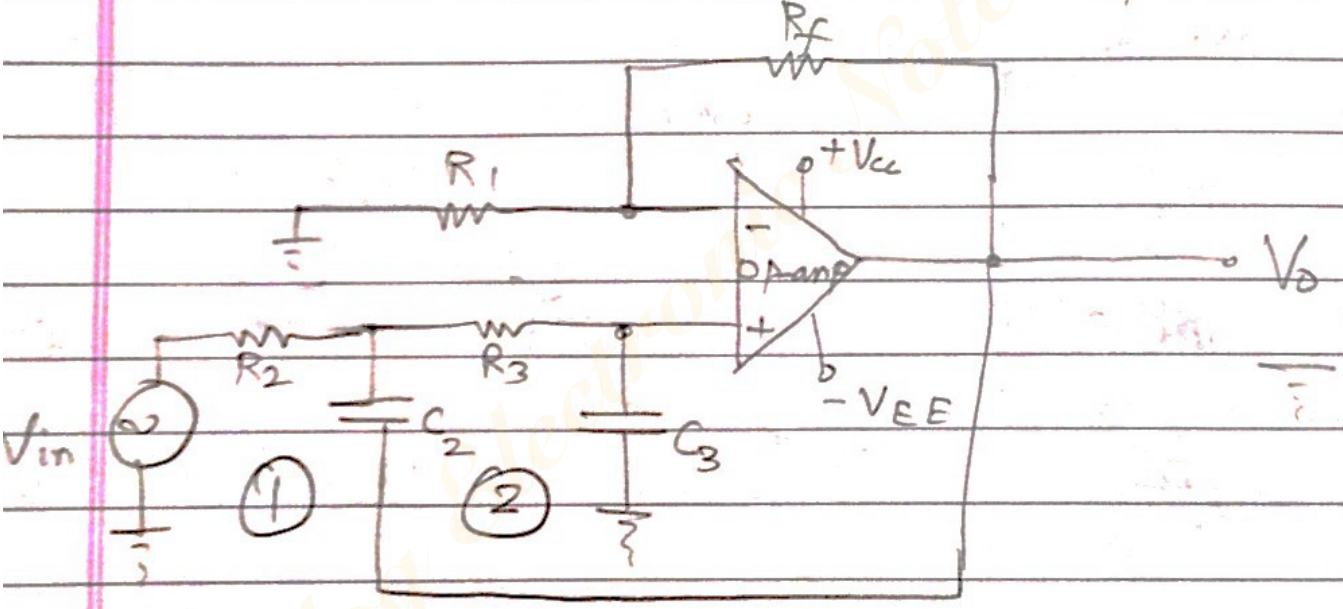
First Order LP Active filter : Butterworth Design.



For 2nd order, add 2 sections of RC at i/p.



✓ We can now find the TF for both order filters.

✓ Analysis can be seen for diff^t values of freq of f.

✓ In above fig, ① & ② are two RC sections for order = 2.

✡ Designing a filter

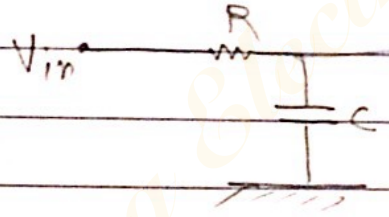
S1) Choose cut off freq, f_H
S2) Choose capacitance C (usually 0.001 to 1 μF)
S3) Estimate req'd value of R.
S4) PB gain is decided by $\frac{R_f}{R_1}$

HW.

① Design a LPF with cut off freq of 15.9 kHz & PB gain = 1.5.
Use 1st order Butterworth filter design.

Analysing RC circuit

Any RC circuit



$$V_A = \left(\frac{X_c}{R + X_c}\right) V_{in}$$

$$V_A = \frac{\left(\frac{1}{j\omega c}\right)}{R + \left(\frac{1}{j\omega c}\right)} V_{in}$$

$$\Rightarrow V_A = \frac{V_{in}}{1 + j2\pi fRC} = \frac{V_{in}}{1 + j\omega RC}$$

let $1/RC = \omega_c$

$$\Rightarrow V_A = \frac{V_{in}}{1 + \frac{j\omega}{\omega_c}} = \frac{1}{1 + (s/\omega_c)} = \text{eqn of 1st order TF.}$$

Now, Finding H(s).

$$\frac{V_o}{V_{in}} = \left(\frac{V_o}{V_A}\right)\left(\frac{V_A}{V_{in}}\right)$$

$\left(\frac{V_A}{V_{in}}\right) \rightarrow \left(1 + \frac{R_f}{R_1}\right)$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{(1 + R_f/R_1)}{(1 + s/\omega_c)} \quad \text{Actual TF}$$

Finding magnitude of TF :-

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1 + (\omega/\omega_c)^2}} \quad \text{(1)}$$

Or $\frac{A_f}{\sqrt{1 + (f/f_H)^2}}$

↳ we write f_H for LPF, ∵ that is the only cut off freq we have ($\omega_c = \omega_H$)

$$f_H = \frac{\omega_H}{2\pi} = \frac{1/RC}{2\pi}$$

$$f_H = \frac{1}{2\pi RC}$$

Finding angle :-

$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right)$$

From (1),

✓ At $f = 0$

$$\left|\frac{V_o}{V_{in}}\right| \rightarrow A_f$$

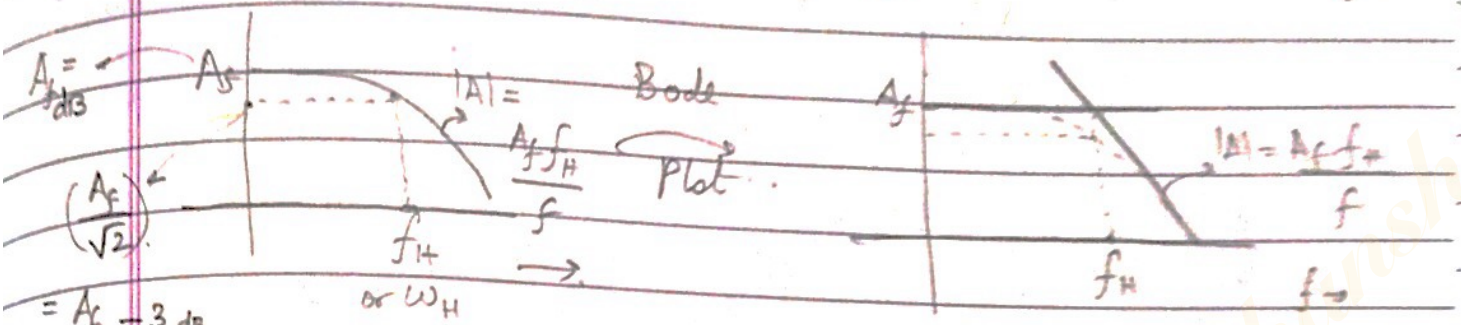
✓ At $f = f_H$.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{2}} \quad (3\text{ dB below } A_f)$$

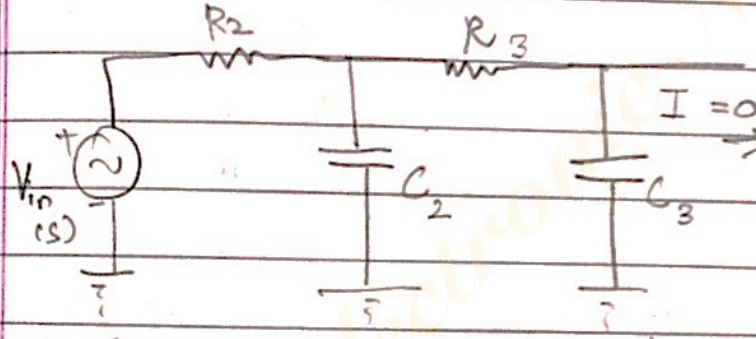
✓ At $f >> f_H$.

$$\left|\frac{V_o}{V_{in}}\right| \simeq \frac{A_f}{\sqrt{f/f_H}^2} \simeq A_f \frac{f_H}{f}$$

So, when $f \uparrow$, $|A| \downarrow$ (hyperbolic decrease of)



2nd Order LP Butterworth Filter :-



Use KVL & KCL to solve this.

Std form :

$$\frac{V_o}{V_{in}} = H(s) = \frac{\omega_c^2}{s^2 + \frac{\omega_c}{Q} s + \omega_c^2}$$

After solving & getting TF, comparing with std. TF,

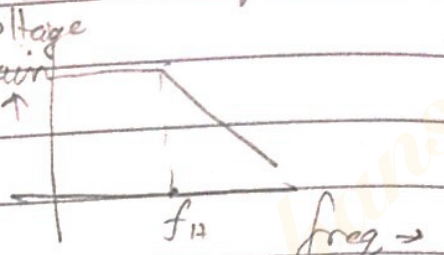
$$\omega_c^2 = \frac{1}{R_2 R_3 C_2 C_3} = \omega_H^2$$

$$\Rightarrow f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

And, $\frac{V_o}{V_{in}} = \underbrace{\left|\frac{V_o}{V_{in}}\right|}_{\text{mag.}} \underbrace{\angle\phi}_{\text{phase}}$

$$\therefore \left|\frac{V_o}{V_{in}}\right| = \frac{A_V}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}}$$ ∵ 2 poles

$\Rightarrow$ Slope $\doteq -40\,dB/dec$



★ Design steps for designing 2nd order filter.

S1) Choose cut off freq f_H.

S2) Simplify by choosing $R_2 = R_3 = R$, $C_2 = C_3 = C$

S3) Choose C in the range $0.001\mu F$ to $1\mu F$.

$$\therefore f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} \rightarrow \frac{1}{2\pi RC}.$$

eg, say design LPF, with $f_H = 10\,kHz$

$$\therefore (10\times10^3) = \frac{1}{2\pi RC}.$$

↳ If $C = 1\mu F$.

$$\Rightarrow (10\times10^3) = \frac{1}{2\pi R(1\mu F)}$$

We can find R and give that value to R_2 & R_3.

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Over TF (actual) 2nd order :-

$$\frac{V_o}{V_{in}} = \frac{A_f}{s^2 + \left(\frac{R_3C_3 + R_2C_3 + R_2C_2 - A_f R_2 C_2}{R_2 R_3 C_2 C_3}\right)s + \frac{1}{R_2 R_3 C_2 C_3}}$$

$$\left(= \frac{\omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \equiv \frac{\omega_c^2}{s^2 + \sqrt{2}\omega_c s + \omega_c^2} \right.$$

↳ $R_2 = R_3 = R$; $C_2 = C_3 = C$, say.

Seeing coeff. of s in denominator

$$\frac{RC + RC + RC - A_f RC}{R^2C^2}$$

$$= \frac{3RC - A_f RC}{(RC)^2} = \frac{3 - A_f}{RC}$$

So, $\frac{3 - A_f}{RC} = \frac{\omega_c}{Q}$ in Butterworth design.

& $\omega_c = \frac{1}{RC}$ & $\frac{\omega_c}{Q} = \sqrt{2}\omega_c$

$\Rightarrow Q = \frac{1}{3 - A_f}$ $\Rightarrow Q = \frac{1}{\sqrt{2}}$

$\Rightarrow \boxed{3 - A_f = \sqrt{2}}$

↳ $3 - A_f = 1.414$

$\Rightarrow A_f = 1.586$.

↳ Std. gain that must be adopted ∀ Butterworth filters

We saw $A_f = 1.586$

For our design, $A_f = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$

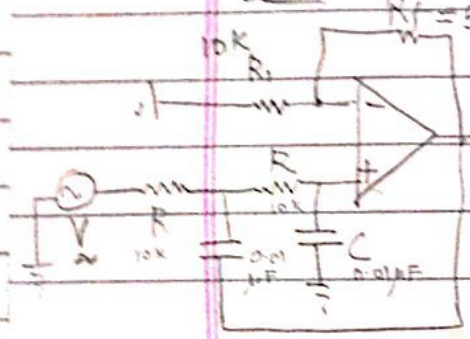
$\Rightarrow \frac{R_f}{R_1} = 0.586$

So, if we take $R_f = 5.86\,k\Omega$ & $R_1 = 10\,k\Omega$.

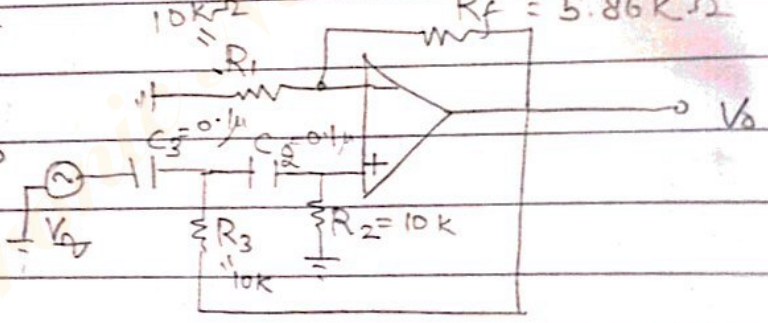
We can get $\frac{R_f}{R_1} = 0.586$

Notes

2nd Order LPF



2nd order HPF



f_H or $f_c = \frac{1}{2\pi RC}$ or $\frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$

f_L or $f_c = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}} = \frac{1}{2\pi RC}$

$A_f = 1 + \frac{R_f}{R_1} = 1.586$

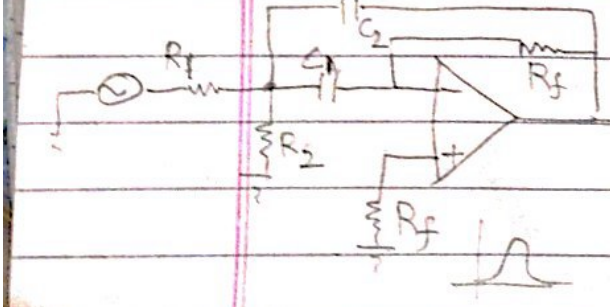
$\frac{V_o}{V_{in}} = \frac{A_f}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}}$

$A_f = 1 + \frac{R_f}{R_1}$, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+(f_L/f)^4}}$

(for 1st ord, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+(f/f_H)^2}}$)

(For 1st ord, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_f(f/f_L)}{\sqrt{1+(f/f_L)^2}}$)

2nd Order BPF (Narrow)



$A_f = \frac{R_f}{2R_1} < 2Q^2$, $R_2' = R_2\left(\frac{f_c}{f_c'}\right)^2$

$R_1 = \frac{Q}{2\pi f_c C A_F}$

$R_2 = \frac{Q}{2\pi f_c C(2Q^2 - A_F)}$

$R_f = \frac{Q}{\pi f_c C}$

For wide BPF,

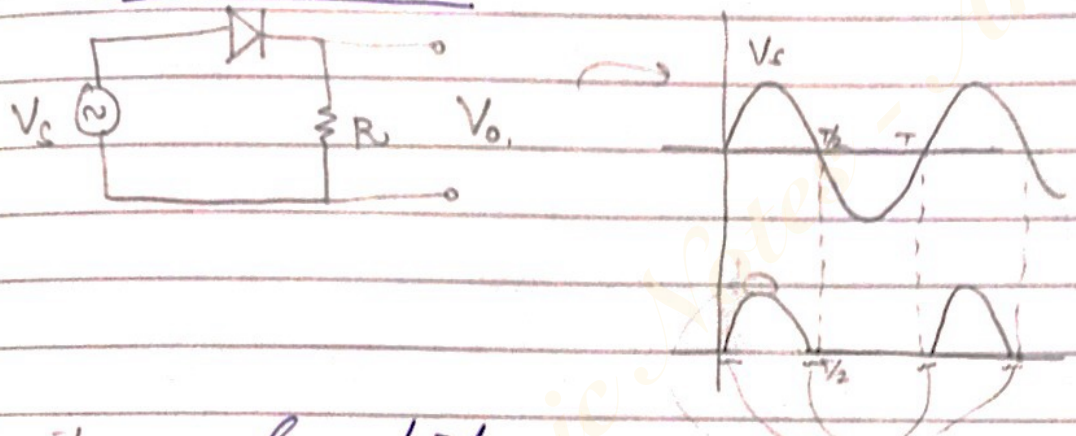
$Q = \frac{f_c}{f_H - f_L}$

$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{F_{total}}(f/f_L)}{\sqrt{(1+f/f_L)^2(1+f/f_H)^2}}$

PRECISION RECTIFIER

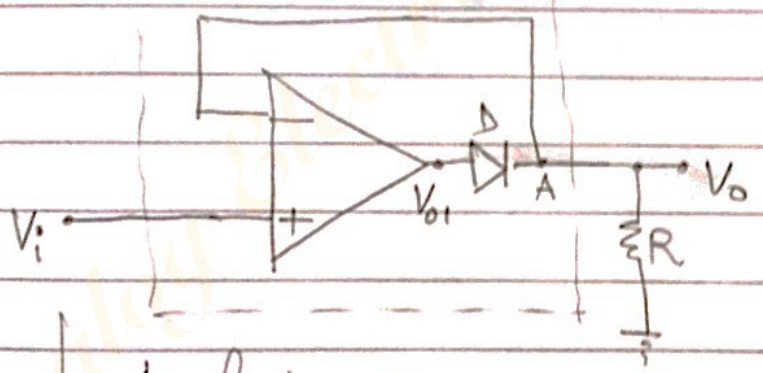
* Note : Every diode has some value of cut-in voltage (that's req^d to turn it (V_γ). Diode can conduct only when the voltage across it is more than V_γ.

HALF WAVE



→ Its not completely half wave rectifier So, we need precision

Consider a Super diode.



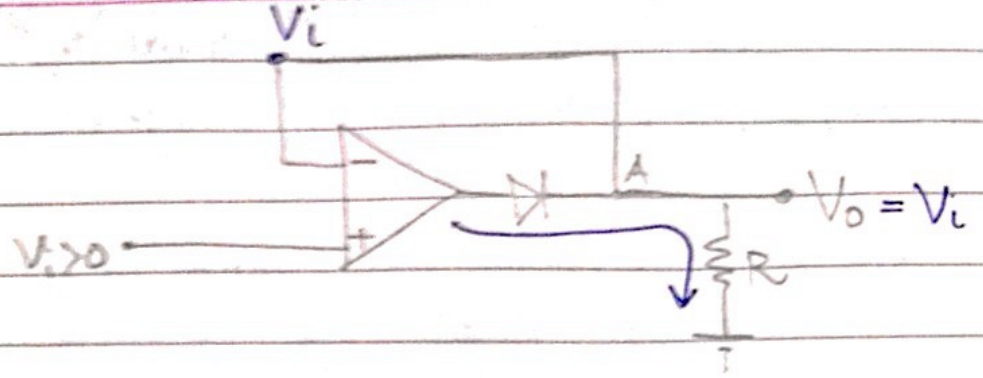
↳ Analysing :

Cases ① $V_i = 0 \Rightarrow V_+ = V_- = 0 \Rightarrow V_A = 0 \Rightarrow V_o = 0$. ⇒ no current flow

② $V_i > 0 \Rightarrow V_+ = V_- > 0 \Rightarrow V_A > 0 \Rightarrow$ current flows across R.

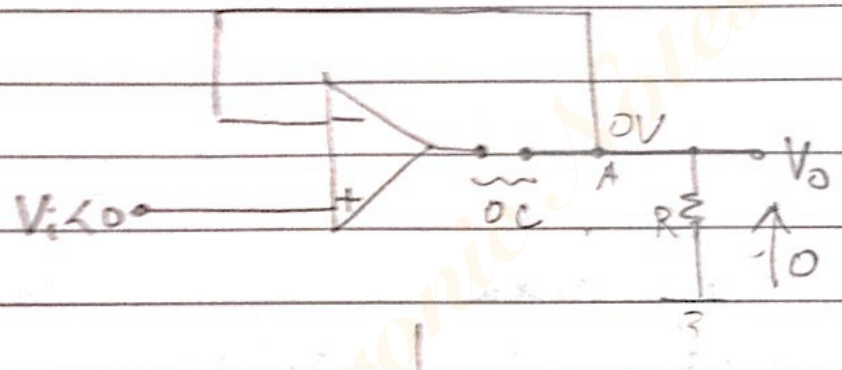
If $V_{diode} = 0.7$ & $V_A = V_i$ Then, we say $V_{01} = V_i + 0.7$

→ where does current come from? → It comes from diode.



③ $V_i < 0$

$\Rightarrow V_+ = V_- < 0 \Rightarrow V_A < 0 \Rightarrow$ GND at higher potential. So, current flows towards diode (tries to flow). Diode blocks. So, $\exists$ no current through resistor



↳ op-amp is driven in satur^n mode

Here, $V_{id} = V_+ - V_- = -ve$.

& $V_{o1} = A\, V_{id} = \infty (-ve) = -\infty$.

So, op-amp will go to satur^n.

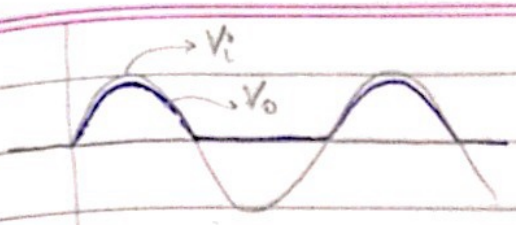
$\therefore V_o = -V_{cc} = -12\ V$.

Including cases ② & ③,

$\Rightarrow$ i/p = +ve, o/p = +ve

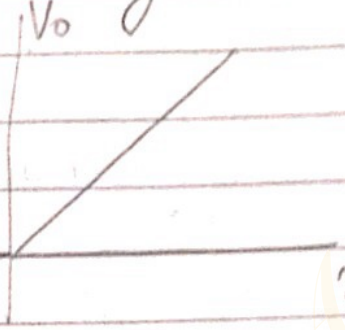
i/p = -ve, o/p = 0.

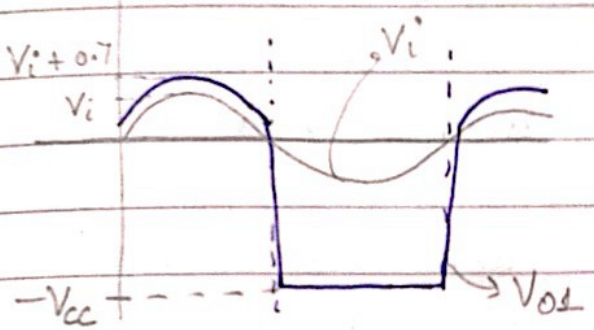
So, it's a COMPLETE half wave rectifier



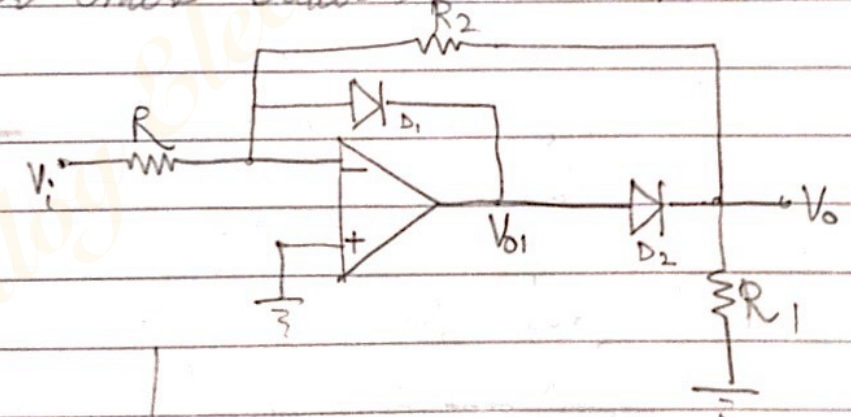
Drawback:
Driving op-amp in saturation for one half cycle

↳ Transfer char.:





Now, we try giving feedback in such a way that op-amp (has) feedback at all times (never enters saturation) → $V_i > 0$ or $V_i < 0$.



Circuit 1

↳ $V_i > 0$ ⇒ current goes through D_1 using that feedback

$V_i < 0$ ⇒ current goes through R_2. So, that feedback is used

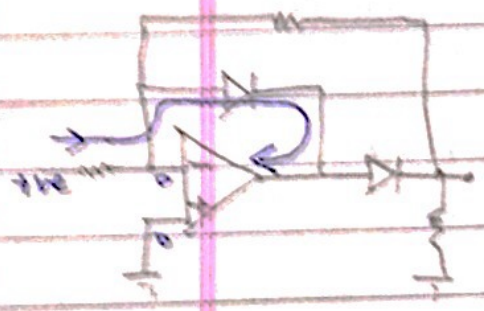
Note: ∵ ∃ feedback V_+ should be equal to V_-.
(won't happen when ~~∃~~ feedback) ⇒ $V_+ = V_- = 0$.

Puffin
Date
Page

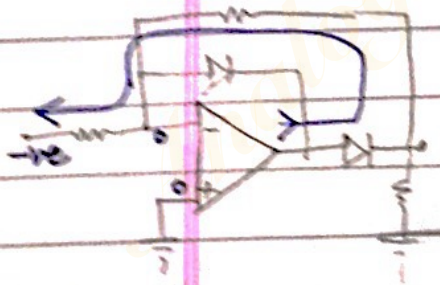
Arguments on Circuit 1

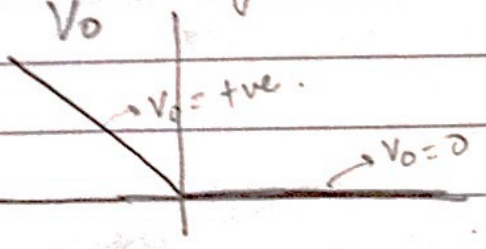
① $V_- = 0$.
(∵ $V_+ = V_-$ at all times, as, ∃ feedback)

② $V_i > 0$
Current doesn't flow through R_2 (∵ D_2 stops it)
Current flows only through D_1
Also, $V_- = 0$ & We have GND near R_1, so, no current flows across R_2.
So, $V_o \simeq 0$
$\Rightarrow V_i > 0 \Rightarrow V_o = 0$

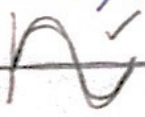


③ $V_i < 0$
Now, current flows across R_2, D_2 (D_1 is inactive)
As current is flowing into op-amp from D_2, $V_- > 0 \Rightarrow V_A$ will be at a lower potential
V_i follows V_o.





* Above circuit is of a Precision rectifier → i.e., it shows o/p at the same instant as i/p comes.

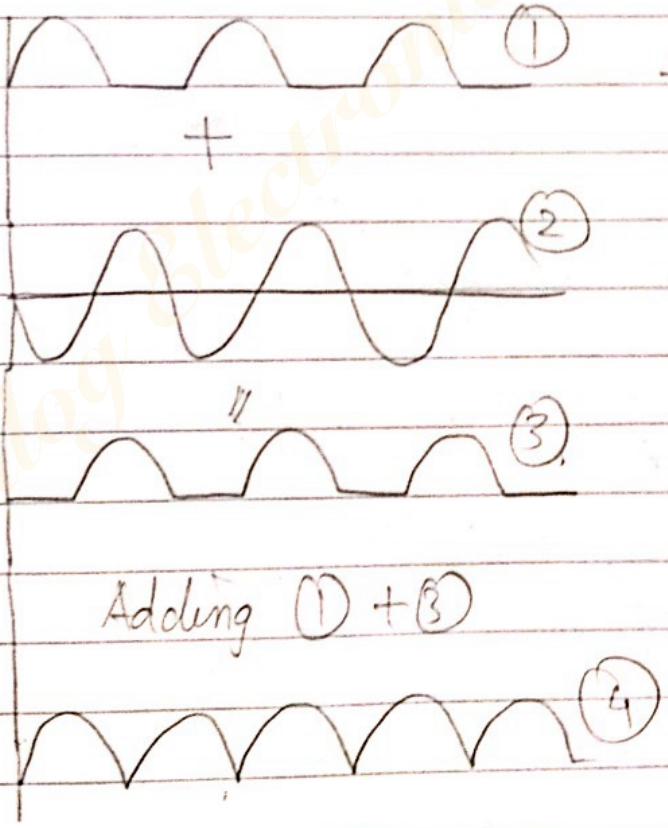


8. FULL WAVE

* Full wave precision rectifiers can be implemented in 2 ways.

① Clubbing two ~~half~~ half wave rectifiers.

Idea: Take one half cycle (①) and add an out of phase (180°) sine wave with it. This will give the other +ve half (②) cycle (③). Now, adding ① + ③ gives a fully rectified output (④).

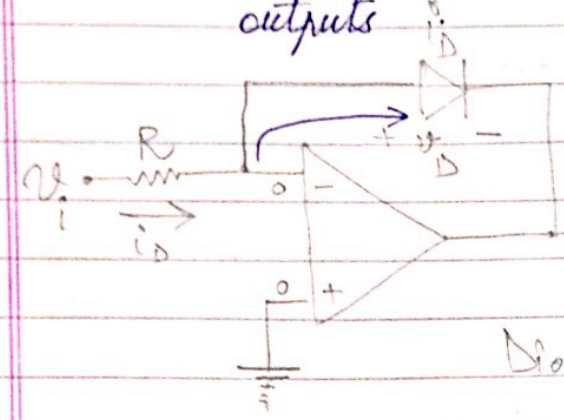


+ve half wave rectifier + Summer + complete sine wave (out of phase 180°)

✡ MULTIPLICATION

Idea :- Multiplic^n in log = Sum in algebra

So, configure op-amp to do logarithmic oper^n. Then, we'll sum the logarithmic outputs



$v_D = -V_o$

Diode eq^n :-

$$i_D = I_s\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right]$$

$$\Rightarrow i_D \simeq I_s \exp\left(\frac{V_D}{V_T}\right)$$

$$\Rightarrow \frac{V_i - 0}{R} \simeq I_s \exp\left(\frac{V_D}{V_T}\right)$$

$$\Rightarrow \frac{V_i}{R} = I_s \exp\left(\frac{V_D}{V_T}\right)$$

$$\Rightarrow \ln\left(\frac{V_i}{I_s R}\right) = \ln\left(\exp\left(\frac{V_D}{V_T}\right)\right)$$

$$\Rightarrow \ln\left(\frac{V_i}{I_s R}\right) = \frac{V_D}{V_T} \longrightarrow -V_o$$

$$\Rightarrow -V_o = V_T \ln\left(\frac{V_i}{I_s R}\right) \longrightarrow \text{Eq}^n \text{ (1)}$$

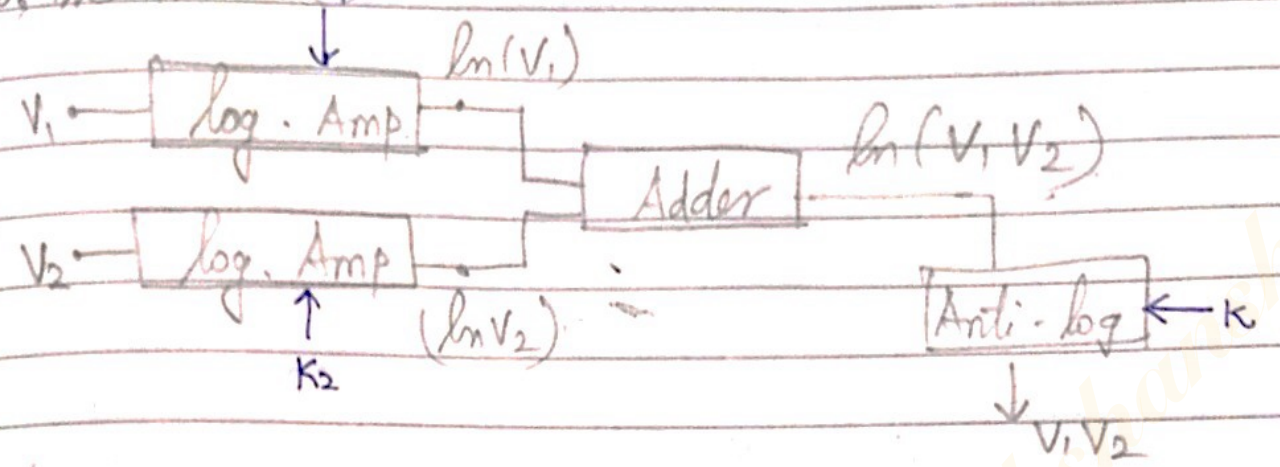
As I_s, R are constants

$\Rightarrow V_o \equiv (\,) \ln(V_I)$

↳ we got logarithmic rel^n

Appropriate → Scaling

So, we have K_1



the block of log Amp. is basically a setup which removes all the constants from eqn (1) (Prev. page)

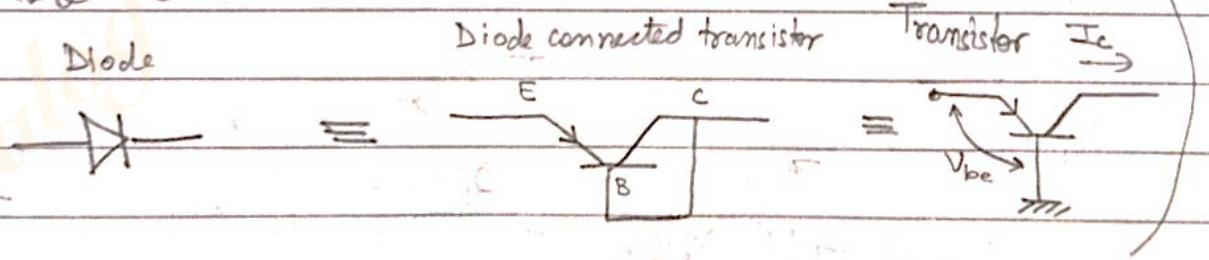
So, we should have

$\checkmark V_0 = \ln(V_i)$ → manage the constants.

Now, once we do that, pass my circuit through Anti-Log Amp. with proper scaling to give

$e^{\ln(V_1 V_2)} = V_1 V_2 \Rightarrow$ Multiplic^n realized.

★ Note :-



eg Consider two signals :

$V_1 = \sin \omega_1 t$

$V_2 = \sin \omega_2 t$

We can now do $V_1 \cdot V_2$.

(If $\omega_1 = \omega_2$ → we have $V_0 = \sin^2 \omega t$)

eg ① Frequency multiplier

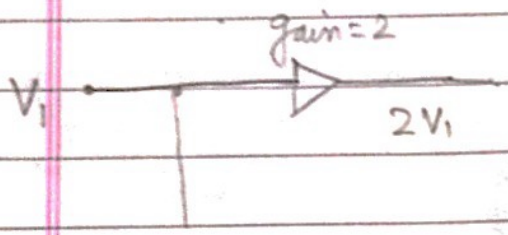
Suppose i/p = $\sin \omega_1 t$

we want o/p = $\sin 2\omega_1 t$

Idea : $\sin 2\theta = 2 \sin\theta \cos\theta$

$= \underbrace{2 \sin\theta}_{2V_1} \underbrace{\sqrt{1 - \sin^2\theta}}$

let $V_1 = \sin\theta$.



① ✓ power ½ → log + antilog

② ✓ $\sin\theta \times \sin\theta$ → multiplier

③ ✓ $1 - \sin^2\theta$ → subtractor

④ ✓ Use ① in ③

eg ② Frequency tripler

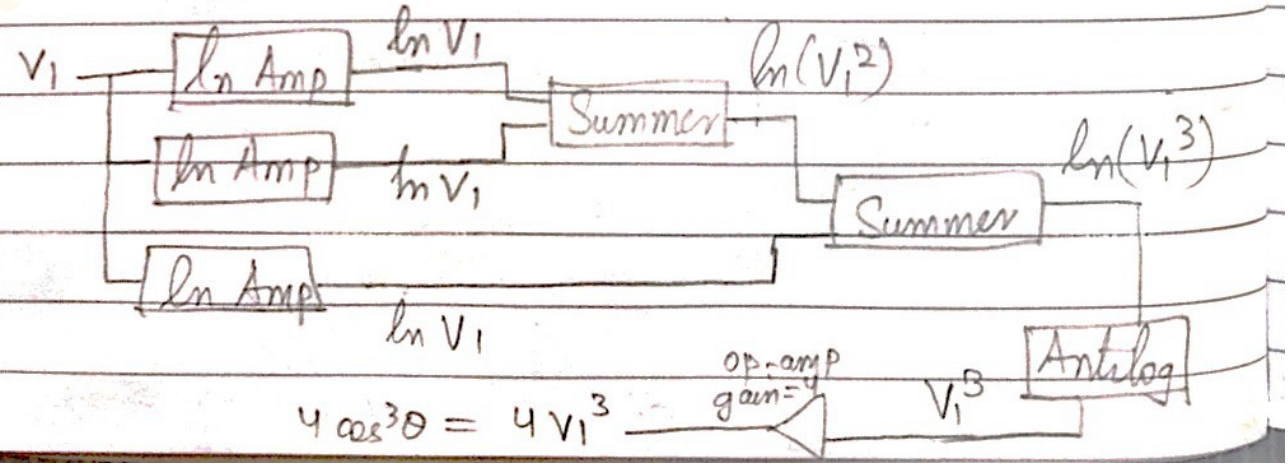
i/p = $V_1 = \cos\theta$

Make o/p = $V_0 = \cos 3\theta$.

Idea :

$\cos 3\theta = \underbrace{4\cos^3\theta}_{\checkmark} - 3\cos\theta$

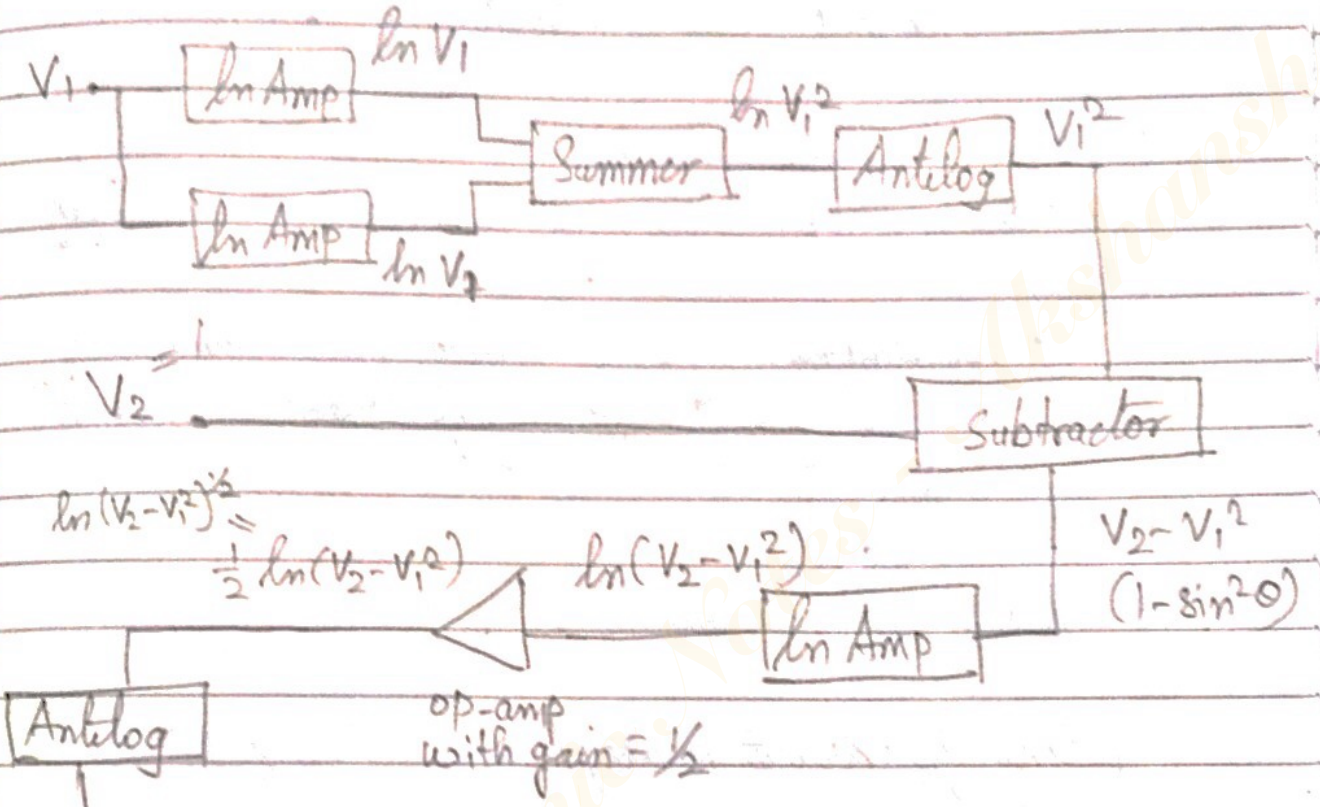
$\underbrace{4 \times \cos\theta \times \cos\theta \times \cos\theta}_{\text{multiplier ⑤}} - \underbrace{3 \times \cos\theta}_{\text{subtractor}}$ (multiplier)



eg ④ Implement $\sqrt{1-\sin^2\theta}$

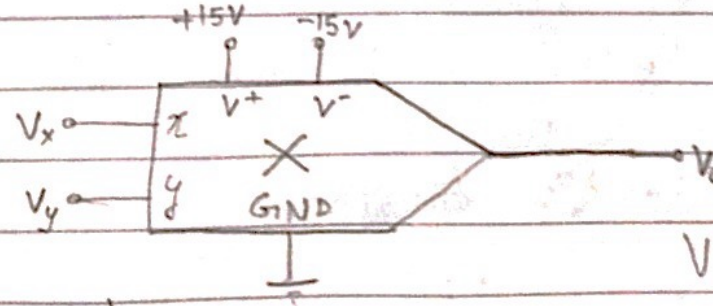
let

$V_1 = \sin\theta$, $V_2 = 1$



(Similar logic can be used to implement anything)

✡ Basic schematic for Multiplier :



$$V_o = \frac{V_x V_y}{V_{ref}}$$

↳ V_{ref} : a constt factor (can be scaled & removed)

* Basically:
Diode (or its equivalent) comes in:
feedback : logarithmic amplifier.
input : anti-log amplifier.

* Note: Implentation of
• Summer or adder : Summing amplifier
(application of Inverting op-amp)
• Subtracter : Difference amplifier
(applic" of non-inverting op-amp)

* Types of multipliers:

1) One quadrant multiplier : $V_x > 0, V_y > 0$

2) Two quadrant multiplier : $V_x = 0, >0, <0$; $V_y > 0$
or $V_x > 0$; $V_y = 0, >0, <0$

3) Four quadrant multiplier : $V_x, V_y = 0, >0, <0$

eg: Frequency Doubler:

If $v_x = V_x \sin\omega t$
$v_y = V_y \sin\omega t$

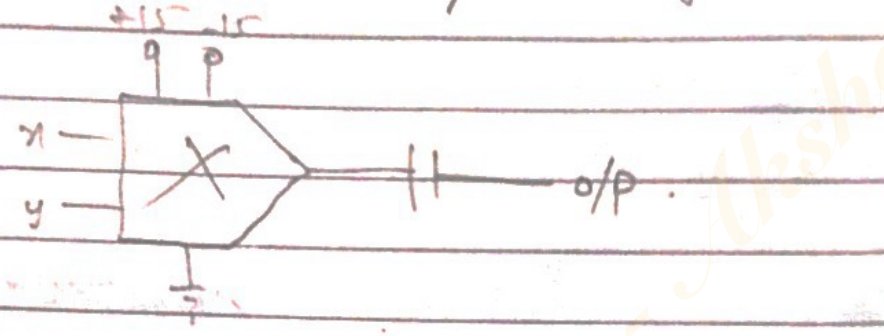
Now,

$$V_o = \frac{V_x V_y \sin^2\omega t}{V_{ref}}$$

$$= \frac{V_x V_y}{V_{ref}} \left(\frac{1 - \cos 2\omega t}{2}\right)$$

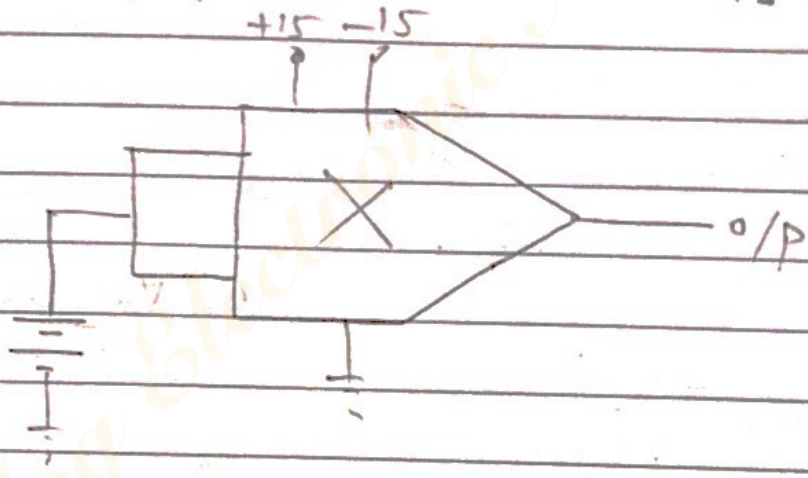
So, V_o has a DC term and a -ve cosine wave of double frequency.

I want only AC. So, remove DC : Use BLOCKING CAPACITOR b/w load and o/p terminal (1 μF Coupling Capacitor)



eg: Frequency Squarer :

Apply same value to both i/p's :-

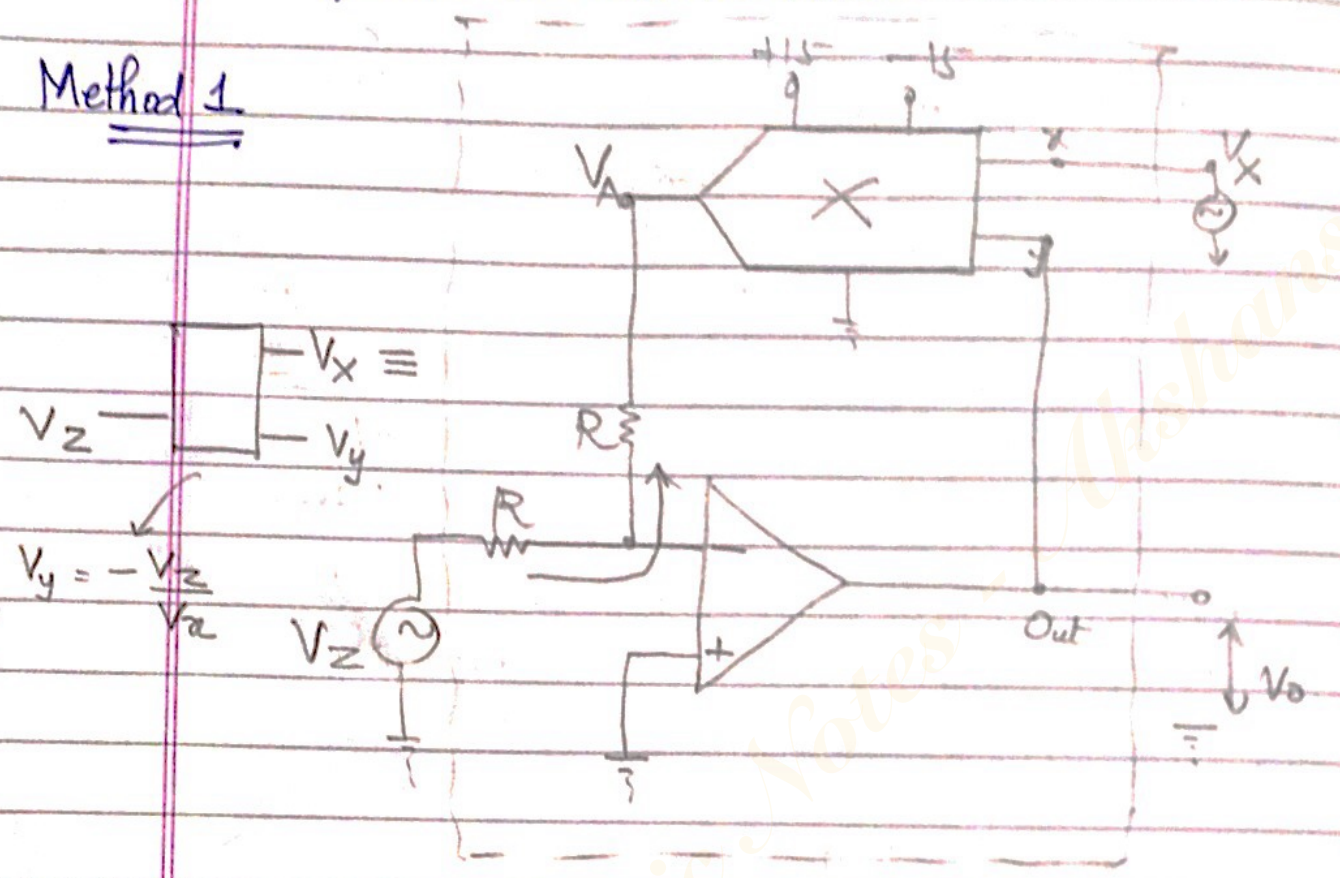


* Note : $\sin\theta \times \sin\theta = \underbrace{\sin^2\theta}_{\text{squarer}} = \underbrace{\frac{1-\cos 2\theta}{2}}_{\text{freq. doubler}}$.

So, a squarer can be seen as freq. doubler

✡ Multiplier as Divider Circuit

Method 1



Notice : This op-amp has a -ve feedback through the multiplier.

$\Rightarrow V_+ = V_-$

$\Rightarrow 0 = V_-$ ($\because V_+ = GND$)

① $V_A = -V_z$

② From multiplier,

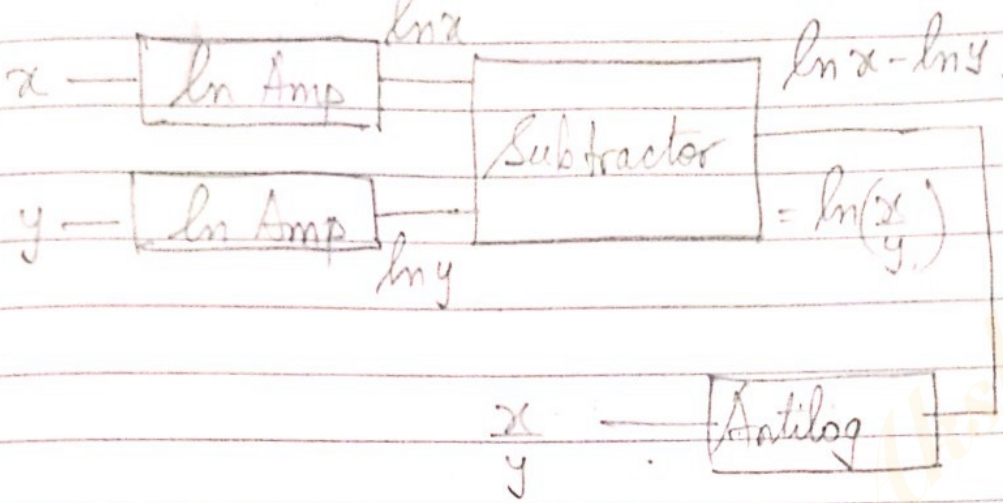
$$V_x \times V_y = -V_z$$

(V_x : i/p, V_y : o/p, V_z : another i/p, $V_z \rightarrow V_A$)

$$\Rightarrow V_y = \frac{-V_z}{V_x} \equiv \frac{(\ )}{(\ )}$$

$\equiv$ Division operⁿ.

Method 2



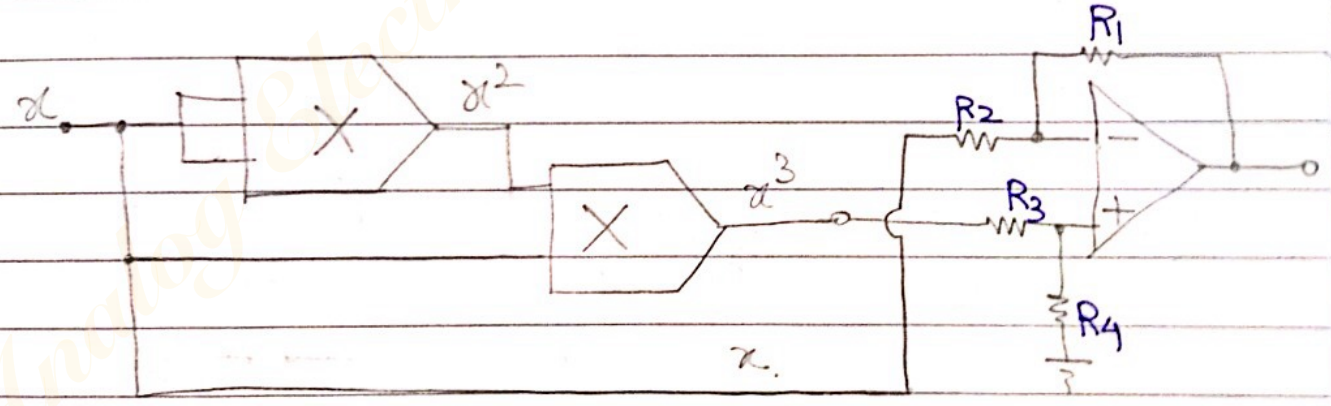
This method is correct, but not used commercially, as std. multiplier circuits are available

eg Implement $\cos 3\omega t$

let $x = \cos \omega t$

$\Rightarrow \cos 3\omega t = 4\cos^3 \omega t - 3\cos \omega t$

$= 4x^3 - 3x$



Note : $\cos^3 \omega t$ term is +ve. So, x^3 goes to non inverting part of difference amplifier & x to inverting part

Note: By POS $\left(\frac{R_4}{R_4+R_3}\right)\left(1+\frac{R_1}{R_2}\right) = 4$ & $-\frac{R_1}{R_2} = 3$.

↳ (1) ↳ (2)

Now, from eqn ②

$\frac{R_1}{R_2} = -3$ So, if $R_1 = 30K\Omega$ & $R_2 = 10k\Omega$

We get o/p = −3 V. (Inverting op-amp part)

Now, from eqn ①.

$$\left(\frac{R_4}{R_3+R_4}\right)\left(1+\frac{30}{10}\right) = 4$$

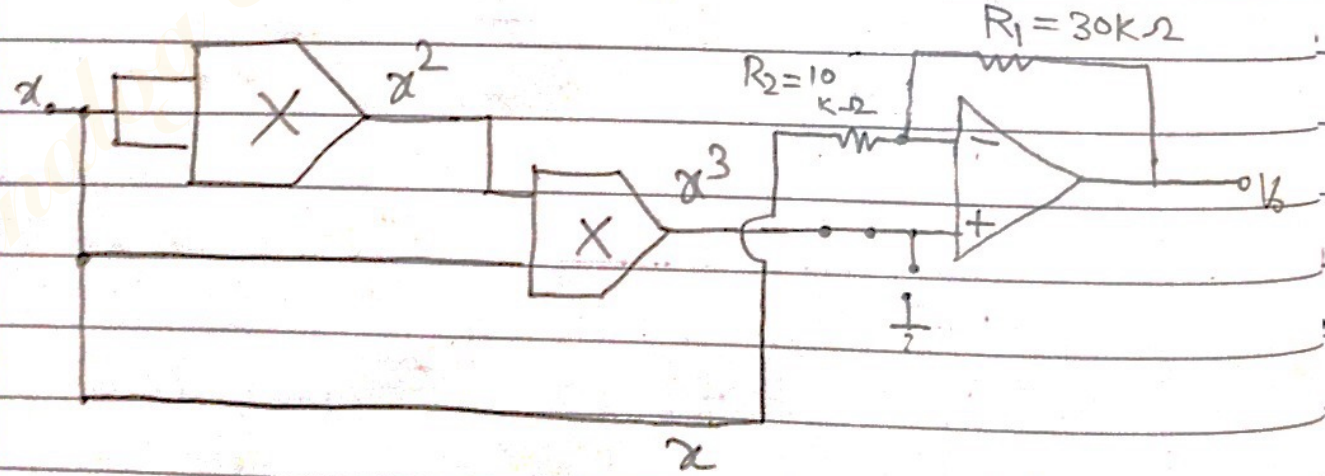
$$\Rightarrow \left(\frac{R_4}{R_3+R_4}\right)(4) = 4$$

$$\Rightarrow \frac{R_4}{R_3+R_4} = 1$$

$\Rightarrow$ R_3 has to be zero.

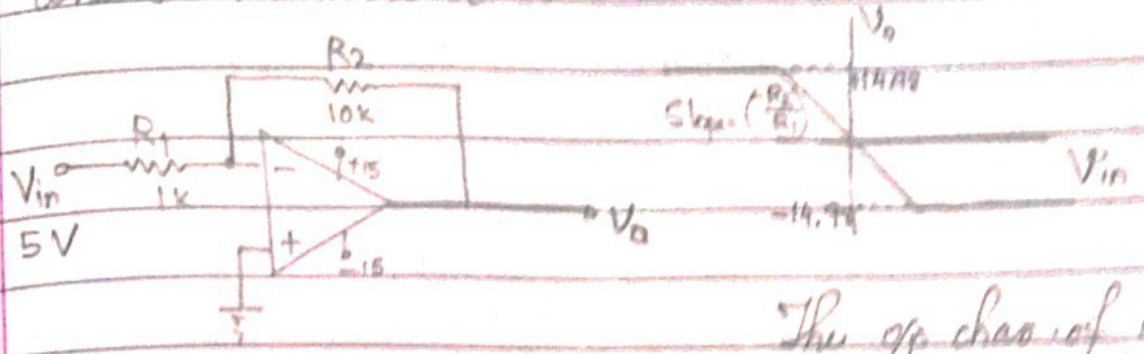
So, short R_3

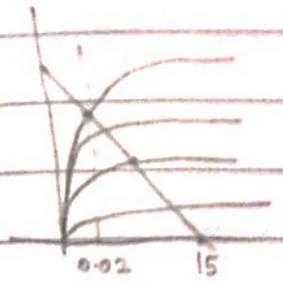
Next, ∵ R_3 is short, R_4 has no meaning. So, Open it. Hence, circuit becomes :



Ans

eg Consider a circuit :





The op char of op-amp is linear in some region & then enters saturation.

V_{SAT} = At saturation $V_o \simeq 15 = 14.98$ (not exactly)

$15 - 0.02$

Note :

At DC

i/p = 5V , expected o/p = -50 → $\left[-5 \times \frac{10}{1}\right]$

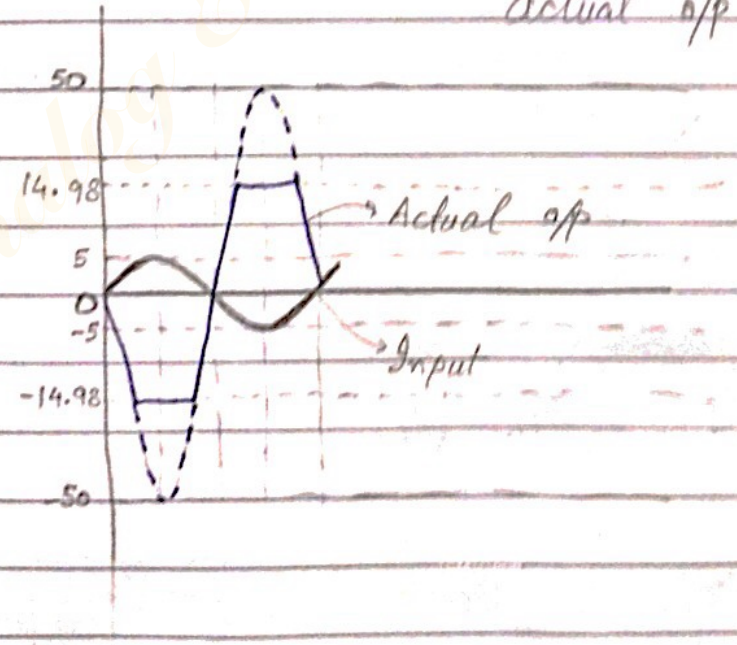
Actual o/p = -14.98

↳ can't go beyond that

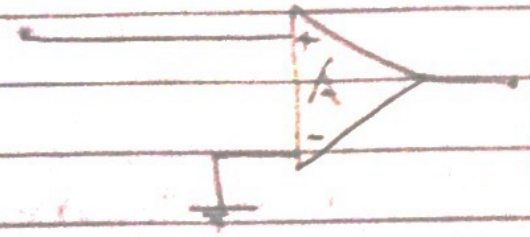
At AC

i/p = $5 \sin \omega t$, expected o/p = $-50 \sin \omega t$

actual o/p = $(-14.98) \sin \omega t$



eg: Consider an op amp 3



$V_{out} = A(V_+ - V_-)$

$\Rightarrow V_{out} = A(V_+ - 0)$

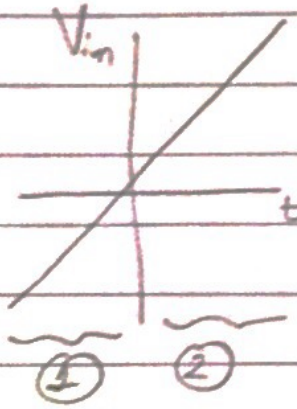
① If V_{in} = -ve.

$\Rightarrow V_{out} = A(-|V_{in}| - 0)$

$= -A|V_{in}|$

$= -15$ cap

o/p cannot be more than $\pm V_{cc}$.



Above circuits were used in digital circuits.

② If V_{in} = +ve.

$\Rightarrow V_{out} = A(+V_{in} - 0)$

$= +15$ cap.

Idea :-

Using of difference amp. as comparator

*Use of threshold levels :

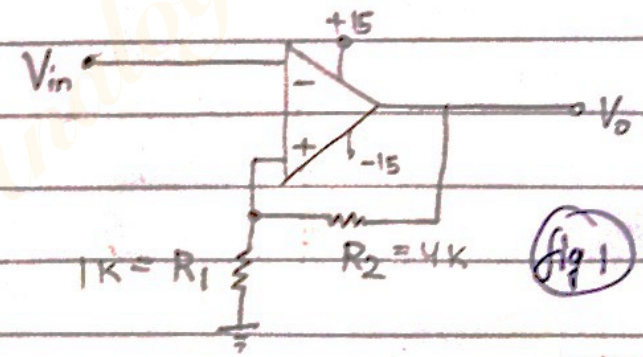


Fig 1

$V_{TH} = \left(\frac{R_1}{R_1+R_2}\right)(\pm V_{SAT})$ ($\pm V_{SAT} = \pm 15$)

$V_{TH} = \pm 3V$.

If I have 2 reference levels in a circuit, Any voltage below one reference level is one state & any voltage above another ref. level is another state. Let reference voltage = V_{TH}

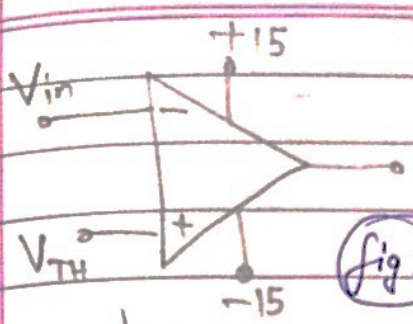


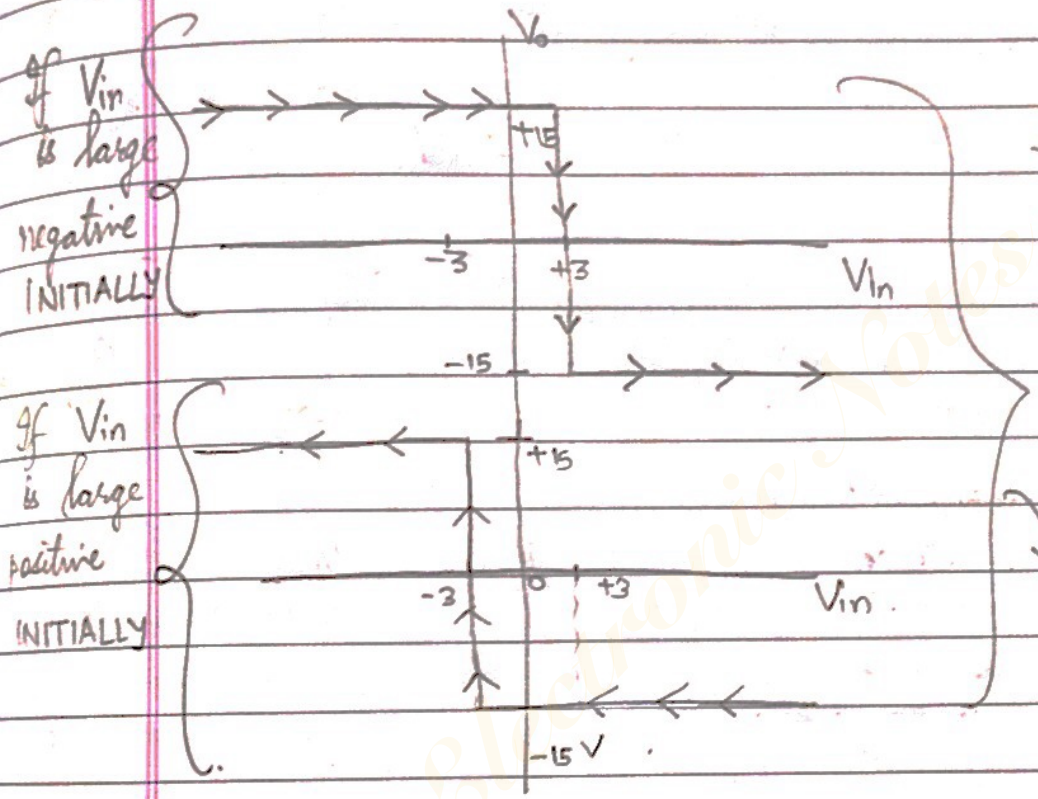
fig 2

$V_{in} > 3V \Rightarrow V_o = -15V$

$V_{in} < 3V \Rightarrow V_o = +15$

↳ let $V_{TH} = 3V$.

(∵ If $V_{in} > V_{th}$, ∃ −ve (+ve)(−ve) saturⁿ. ↳ inverting op-amp)



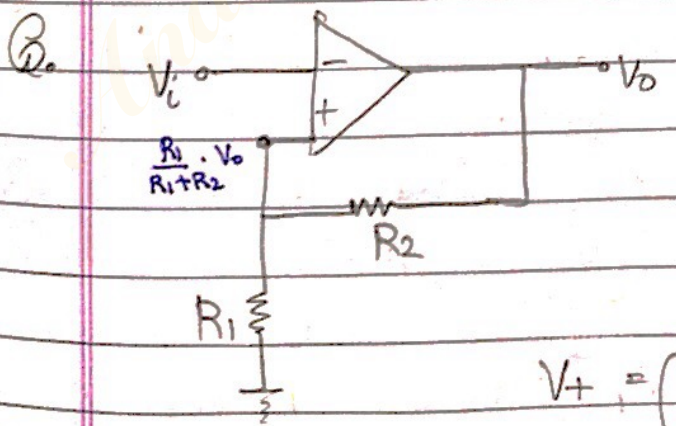
+3V is the threshold pt.

$V_{in} < 3 \Rightarrow +15$ V

$V_{in} > 3 \Rightarrow -15$ V

→ HYSTERESIS

Q.



This is the circuit of a comparator.

It has a +ve feedback.

↳ (V_o) o/p will be $+V_{SAT}$ or $-V_{SAT}$ depending on i/p.

$V_+ = \left(\frac{R_1}{R_1+R_2}\right) V_o$ ≡ THRESHOLD LEVEL to compare with V_i

Suppose V_i is large negative $\Rightarrow V_-$ is large -ve

& we know, $(V_+) - (V_-) A = V_o$

↳ (small value) − (large -ve value) = +ve value

↳ A is very large

$\Rightarrow V_o = +V_{SAT}$

Suppose V_i is large positive

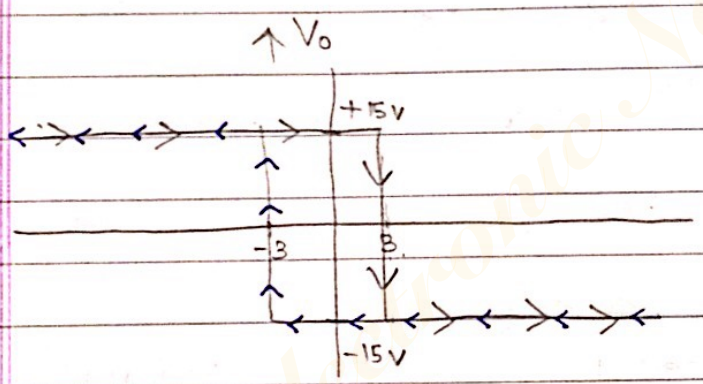
$\Rightarrow$ V_- is large positive ($\approx +V_{SAT}$)

$\Rightarrow V_o = +V_{SAT}$

Now, if $R_2 = 4$, $R_1 = 1 \Rightarrow V_+ = \left(\frac{1}{5}\right) V_o$.

At large -ve V_i, $V_+ = \frac{1}{5}(+15)$

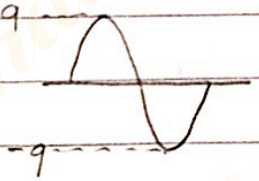
$\Rightarrow V_+ = +3\ V$



O/p continues to remain at +15 V until upper threshold (+3 V) is reached

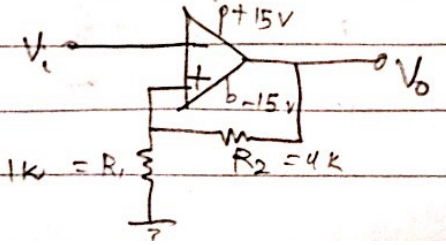
O/p will remain steady even though ∃ fluctuation at i/p.

eg



i/p = 9 sin ωt

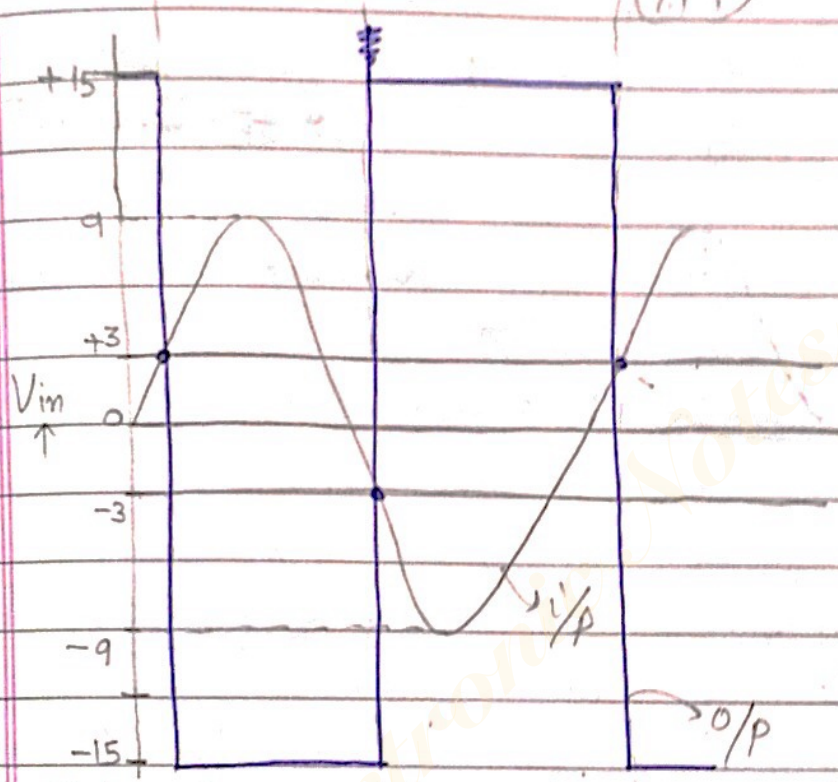
Determine waveform at o/p for a comparator circuit:



S1) Find the threshold voltage (at V_+) i.e that is compared with V_-.

(UTL) Upper threshold :- $\left(\frac{1}{1+4}\right) 15 = 3V$.

(LTL) lower threshold :- $\left(\frac{1}{1+4}\right)(-15) = -3V$



S2: Mark the input

S3) Make UTL & LTL on graph.

- & mark switch over points on graph.

Now, see the o/p by taking the switch over points at $\pm V_{SAT}$

This is called Schmdt Trigger.

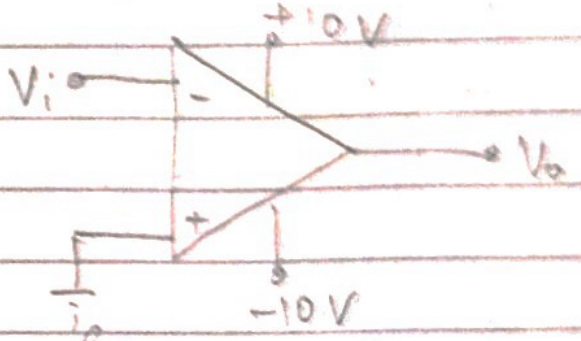
So, analog i/p → digital o/p.

Note :- If i/p = 2 sinωt, threshold is ± 3V,

So, we wont cross threshold at anytime.

So, no switching. +15V always.

* Simple comparator (seen before)



Q: Find V_o when $V_i = -2$ V.

Ans:- We know

$$(V_+ - V_-)A = V_o$$

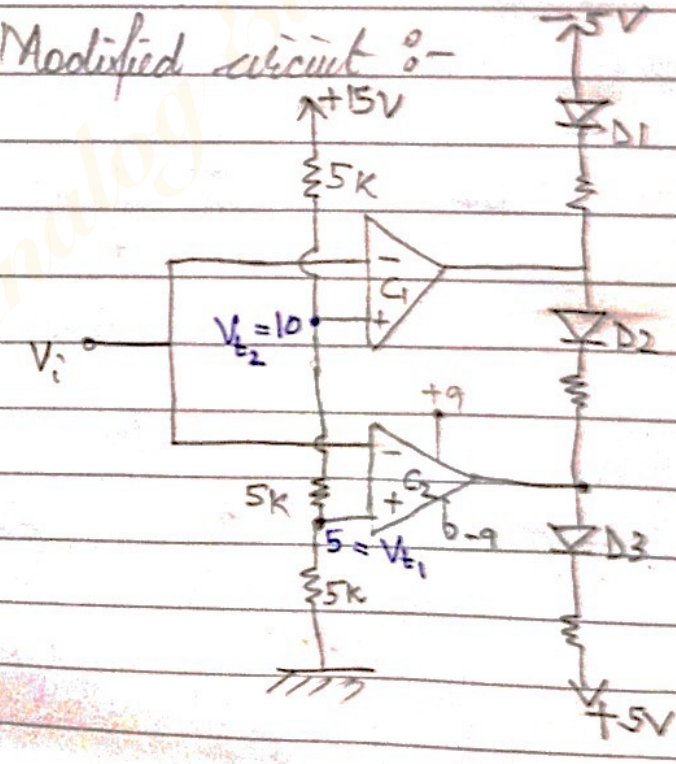
$V_+ \to 0$, $V_- \to -2$

$A(+2)$ = very large. So, o/p will be very large. But it can't exceed its i/p, o/p V_o = 10 V

If the signal crosses zero with $V_i = \pm 2$ V, then $V_o = -10$ V.

So, any crossing from 0V can be detected

eg Modified circuit :-

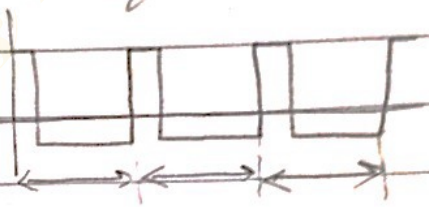


If i/p = b/w 0-5V
C_2 will give o/p is +5 V.
So, for D1, D2, D3, +9 to +5 & FB
=) if 'll flow
Two top leds will glow.

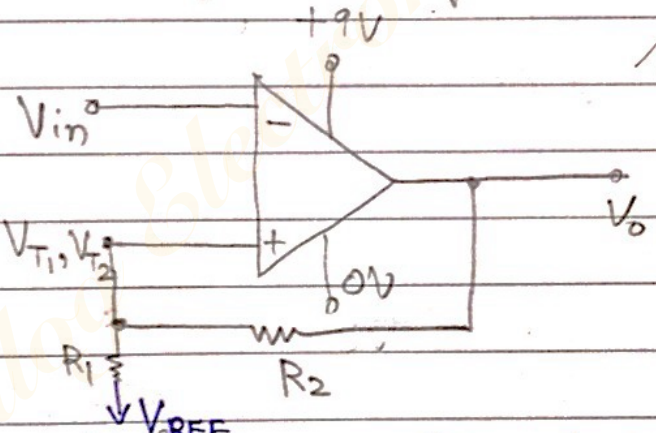
If i/p is at $-10\,V$,
C_2 gives out $-9\,V$. So, D_3 doesn't glow.
C_1 gives out $+9\,V$
So, D_2 glows & D_1 doesn't glow.

Note: As we have $\pm V_{SAT}$, we will have $\pm V_{th}$.
"satur" threshold

So, we will get a symmetric shape.
Unsymmetrical Square wave: A sq. wave with duty cycle NOT 50%.
→ $T_{ON} \neq T_{OFF}$



Q: Design:
Schmitt trigger with unsymmetric voltage levels?



here, $+V_{SAT} \simeq < 9\,V$
$= 8.5\,V$, say.
$-V_{SAT} \simeq 0.5\,V$, say

Idea: Make a comparator s.t 2 threshold limits are non symmetrical.
So, { UTL = 7V & LTL = 6V } say.

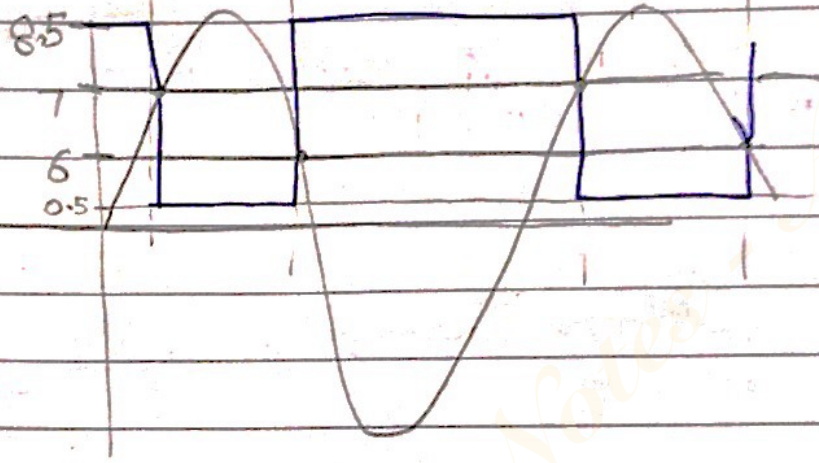
Find V_{REF}, R_2, R_1 s.t, $V_{T_1} = 6\,V$, $V_{T_2} = 7\,V$
2 threshold levels

Now, when $V_o = 8.5\,V$, $V_{T_1} = 7\,V$.

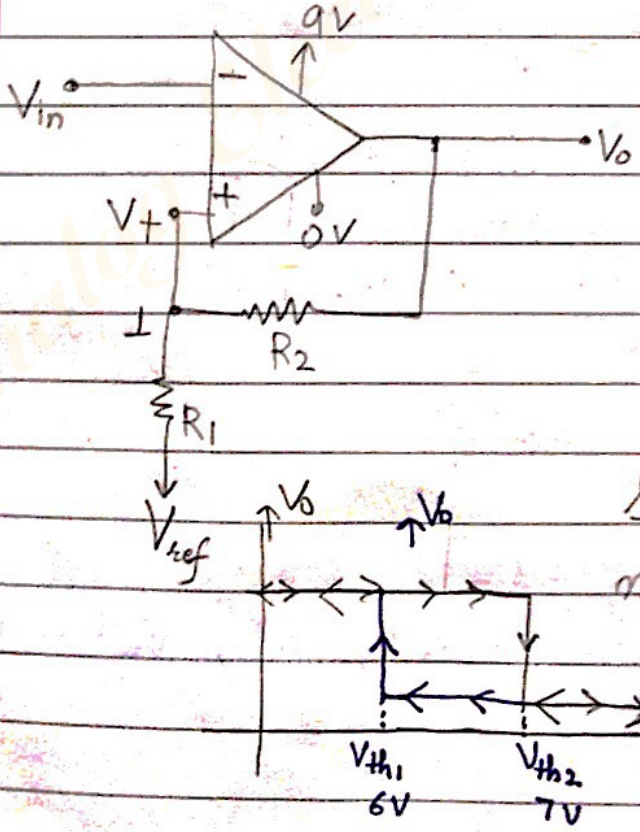
$V_o = 0.5\,V$, $V_{T_2} = 6\,V$.

Using these 2 expressions to find values of V_{R_1}, R_2, V_{REF}

↳ after computation : $V_{REF} \simeq 6.79\,V$



Q. ✱



Consider an OP-AMP working on a SINGLE power supply.

Given :-

$+V_{SAT} = 8.5\,V$

$-V_{SAT} = 0.5\,V$.

Since, it's a comparator, make the circuit behave as:

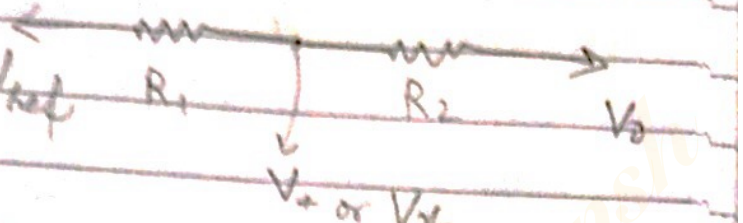
i.e.,

Find value of R_1, R_2, V_{ref}.

Values will depend on V_+

So, finding V_+

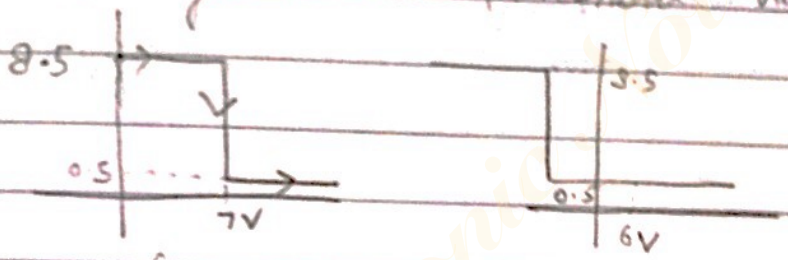
Idea: ∃ 2 sources of voltage :) Use POS



$$\Rightarrow \left(\frac{R_1}{R_1+R_2}\right)V_0 + \left(\frac{R_2}{R_1+R_2}\right)V_{ref} = V_x$$

V_x → +ve or -ve threshold

From ✓ fig, when o/p changes, saturⁿ level changes. Our threshold values are 6V & 7V.



(Upper saturⁿ level) (Lower saturⁿ level)

Eqn by POS:

$$V_{TH} = 7 = \left(\frac{R_1}{R_2+R_1}\right)(8.5) + \left(\frac{R_2}{R_1+R_2}\right)V_{ref}$$

$$V_{TL} = 6 = \left(\frac{R_1}{R_1+R_2}\right)(0.5) + \left(\frac{R_1}{R_2+R_1}\right)V_{ref}$$

↳ subtracting

$$\Rightarrow 1 = 8\left(\frac{R_1}{R_1+R_2}\right)$$

$$\Rightarrow R_1+R_2 = 8R_1 \quad \text{or} \quad R_2 = 7R_1$$

Solve $\Rightarrow 7 = \frac{8.5}{1+7} + \frac{1}{(1+1/7)}V_{ref}$

$\Rightarrow V_{ref} \simeq 6.79\,V$

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The proportion of R_1 & R_2 values to go in 0's & 1's

eg :- If $R_2 = 70K$; $R_1 = 10K$ follows the ratio

The proportion of R_1 & R_2 values to go in Op-Amp's

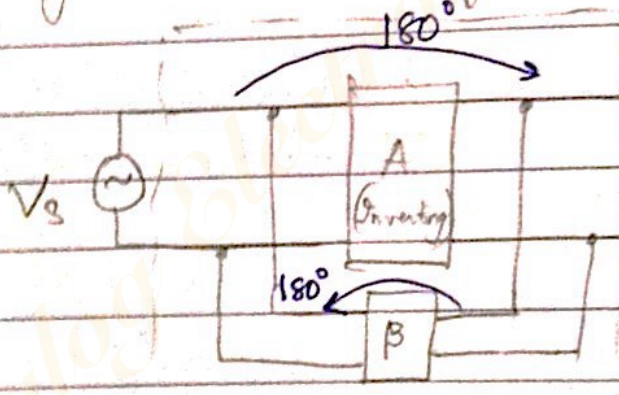
eg:- If $R_2 = 70K$; $R_1 = 10K$ follows the ratio

✡ SIGNAL GENERATORS

↳ Allow to generate any type of signal: sinusoidal, square and triangular.

eg: Schmitt trigger for generating Sq. wave

If I have something like this:



Note:-

$(V_s + \beta V_o) A = V_o$

$\Rightarrow V_s A + A\beta V_o = V_o$

$\rightarrow V_s A = (1 - A\beta) V_o$

So, $A_f = \frac{V_o}{V_s} = \frac{A}{1 - A\beta}$.

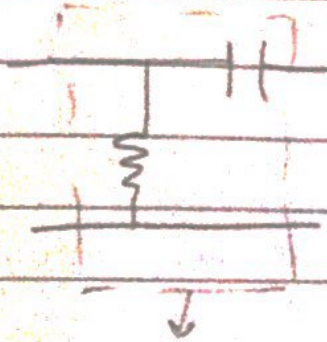
↳ If $|A\beta| \approx 1 \Rightarrow A_f \rightarrow \infty$.

* Condition for Circuit to give OSCILLATION :
$|A\beta| = 1$ & $\angle A\beta = 0$: BARKHAUSEN Criterion

* To change freq of oscil^n, change resistance of capacitor in circuit

* Total phase change through the circuit is 360° (180° + 180° ≡ 0(°))

If β circuit is seen as an RC network



So,

$$T(s) = \frac{R}{R + X_c} = \frac{R\angle 0°}{\left(R + \frac{1}{j\omega C}\right)}$$

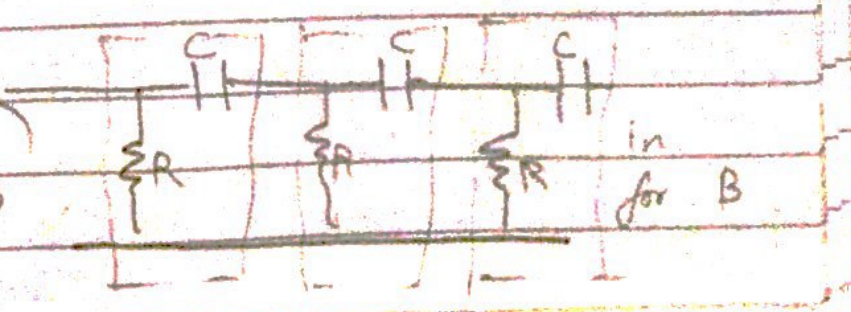
$$\left|\sqrt{R^2 + \frac{1}{\omega^2 C^2}}\right| \quad \angle \tan^{-1}\left(\frac{1}{\omega CR}\right)$$

So, Phase shift due to one RC network $= -\tan^{-1}\left(\frac{1}{\omega CR}\right)$

$\simeq 60°$

So, put 3 RC networks ($\simeq 180°$)
Now we got 180° by feedback part making total of 0°

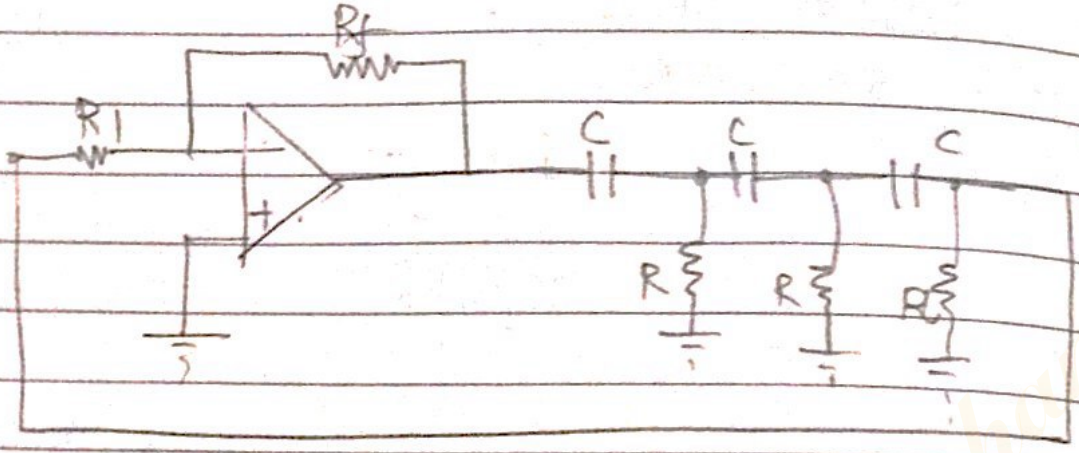
Something like :-



for this,

$|A\beta| = 1$

✱ Phase shift network



↳ Change R_1 to get Gain of Value $\frac{1}{\beta}$

By analysis, we can get

$$f = \frac{1}{2\pi RC\sqrt{6}}$$ (PTO, for details)

$$|\beta| = \frac{-1}{29}$$

& $|A| = 29$

✱ Advantages & Disadvantages of Phase Shift Oscillator.

Advantage ✓ Deals with single freq

Disadvantage ✓ R should be changed instead of C. But, All R's will have to be changed

---

HW Q. Design a phase shift oscillator to have o/p freq of 500 Hz. Use ± 12 V Supply

(Done later)

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Analysis (in brief)

$$\beta = \frac{V_o}{V_i} = \frac{R^3}{(R^3 - 5RX_c^2) + j(X_c^3 - 6R^2X_c)}$$

↳ for 180° phase shift of β-network

$\angle A\beta = 0$

⇒ no imaginary component

⇒ $X_c^3 - 6R^2X_c = 0$

↳ $X_c = 0$ → Rejected.
(0°C cannot be infinite)

↳ $X_c^2 = 6R^2$

⇒ $X_c = \pm\sqrt{6}R$

(Capacitance cannot be -ve, so take +ve only)

⇒ $X_c = \sqrt{6}R$

⇒ $\frac{1}{\omega C} = \sqrt{6}R$

⇒ $\omega = \frac{1}{\sqrt{6}RC}$

⇒ $f = \frac{1}{2\pi\sqrt{6}RC}$

↳, now, $\beta = \frac{R^3}{R^3 - 5RX_c^2}$

↳ Put $X_c = +\sqrt{6}R$

⇒ $\beta = \frac{R^3}{R^3 - 5R(6R^2)}$

⇒ $\beta = \frac{\ominus 1}{29}$ → 180° phase shift

Now, $A\beta$ should be $\perp$

As $\beta = \frac{-1}{29}$ or $|\beta| = \frac{1}{29}$

So, $A = 29$

(Satisfying Barkhausin's Criterion)

HW Problem.

Sol^n f is less than 1 kHz. Use μA-741 op-amp

$I_b(max) = 50\,nA$

$I_1 = 100\, I_b(max) = 5\mu A$

$R_f = \frac{V_o(sat)}{I_1} \rightarrow V_o(sat) = 12 - 1 = 11\ V.$

$= \frac{11}{5 \times 10^{-6}}$

$\Rightarrow R_f = 2.2\,M\Omega$ (Std. value)

Now, $A_{CL} = \frac{R_f}{R_1} \geq 29$

$R_1 = \frac{R_f}{29}$

$\Rightarrow R_1 = 75.8 \times 10^3\ \Omega$, $R_f = 2.2\,M\Omega$

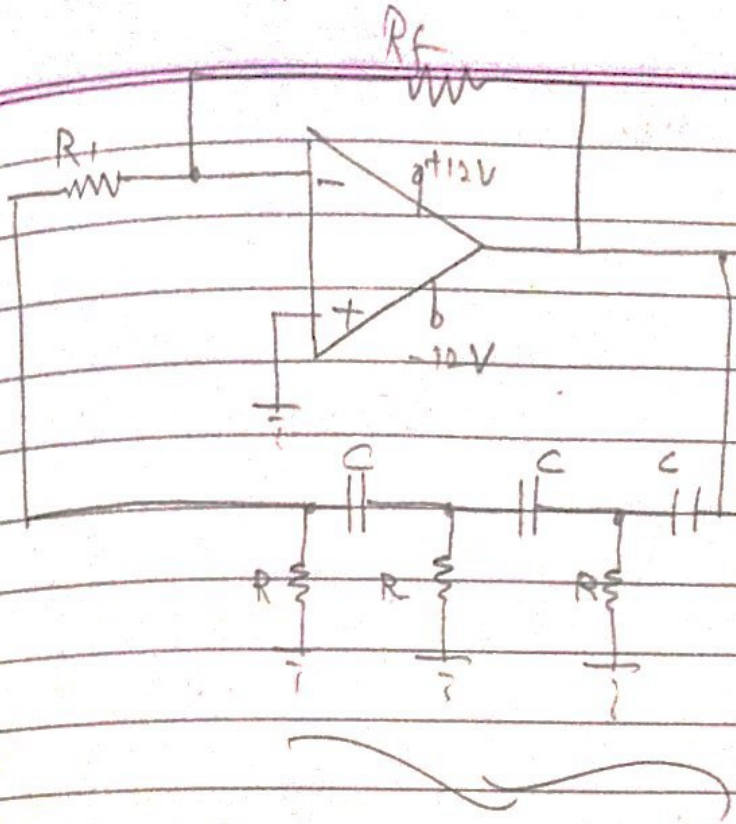
Design rule, in my RC network

$R = \frac{R_1}{10} = 7.5\,k\Omega$ (Std. value)

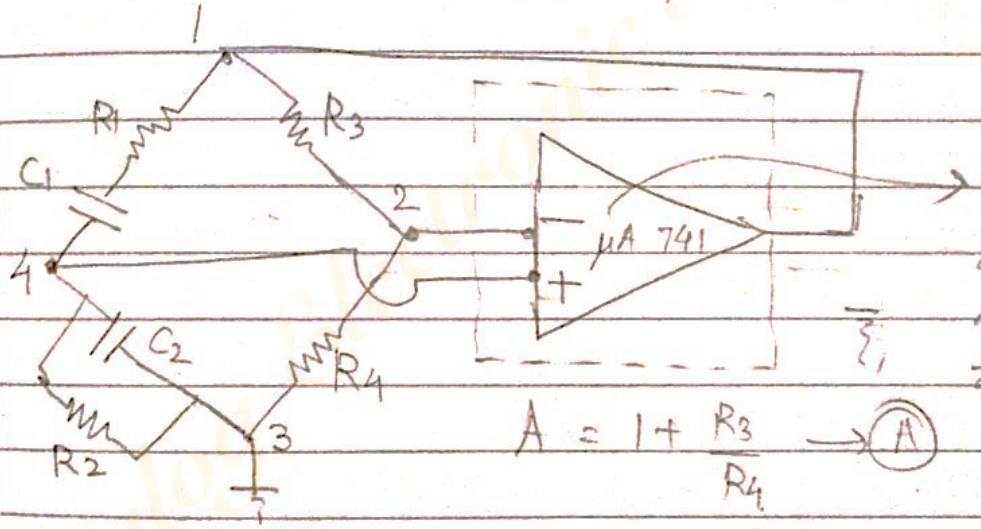
C : on the basis of freq.

$= 0.0017\,\mu F$.

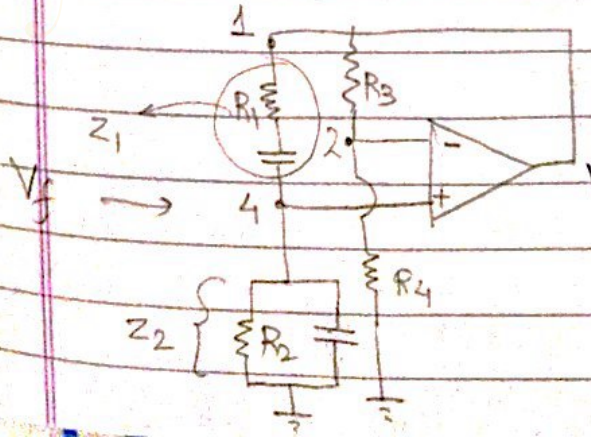
* CE Amp gives 180° phase shift. But 2 CE stages in series can give 0° phase shift



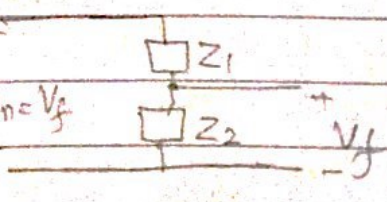
* Wein Bridge (Unlike previous ~~A~~ phase shift, $\angle AB = 0$)
$\angle A = 0$ & $\angle B = 0$



$$A = 1 + \frac{R_3}{R_4} \rightarrow (A)$$



$$V_f = \left(\frac{Z_2}{Z_2 + Z_1}\right) V_o \rightarrow (B)$$



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Part 1 Solving to make $\angle\beta = 0$ (i.e., imaginary part = 0)

$$\beta = \frac{\omega^2 C_1 R_2 (R_1 C_1 + R_2 C_2 + C_1 R_2) + j\omega C_1 R_2 (1 - \omega^2 R_1 R_2 C_1 C_2)}{(1 - \omega^2 R_1 R_2 C_1 C_2)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + C_1 R_2)^2}$$

↳ Comes after Putting $s = j\omega$. Now, removing all imaginary components

↳ $\omega (1 - \omega^2 R_1 R_2 C_1 C_2) = 0$

↳ $\omega \neq 0$ (∵ DC ✗)

↳ $\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$

-ve value of ω can't be there ← $\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$

$$\Rightarrow f = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

freq of oscill^n of this circuit

↳ $R_1 = R_2$, $C_1 = C_2$ in practical circuits

$$\Rightarrow f = \frac{1}{2\pi RC} \quad \text{or} \quad \omega = \frac{1}{RC}.$$

Now, on taking $\omega = \frac{1}{RC}$.

$R_1 = R_2$, $C_1 = C_2$

$$\beta = \frac{\omega^2 RC(3RC) + j\omega RC(1 - \omega^2 R^2 C^2)}{(1 - \omega^2 R^2 C^2) + \omega^2 (3RC)^2}$$

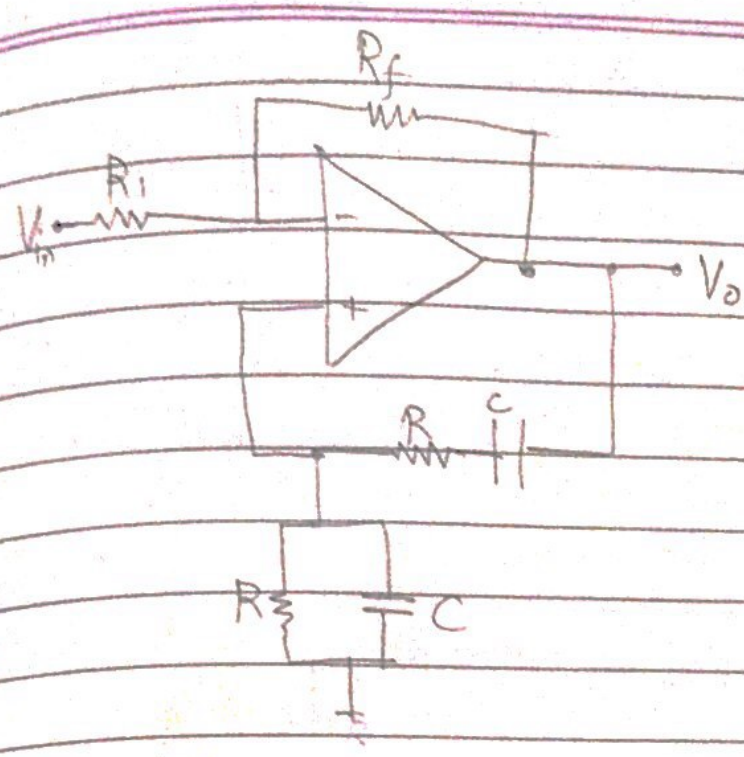
↳ $\omega = \frac{1}{RC}$ (freq of oscill^n as got)

$$\Rightarrow \boxed{\beta = \frac{1}{3}}$$

So, for making $A\beta = 1$, $\boxed{A = 3}$

Now, $A = 1 + \frac{R_3}{R_4} = 3$

$\Rightarrow \frac{R_3}{R_4} = 2 \Rightarrow R_3 = 2R_4$ or $\boxed{R_3 = 2R_1}$



Simplified Wein Bridge, with $R_1 = R_2$, $C_1 = C_2$

eg Design Wein bridge oscillator to have o/p freq of 10 kHz

Choose $C = 0.01\,\mu F$

$$R = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$R = 1.59\,k\Omega$

↳ Choose Std. value $= 1.5\,k\Omega$

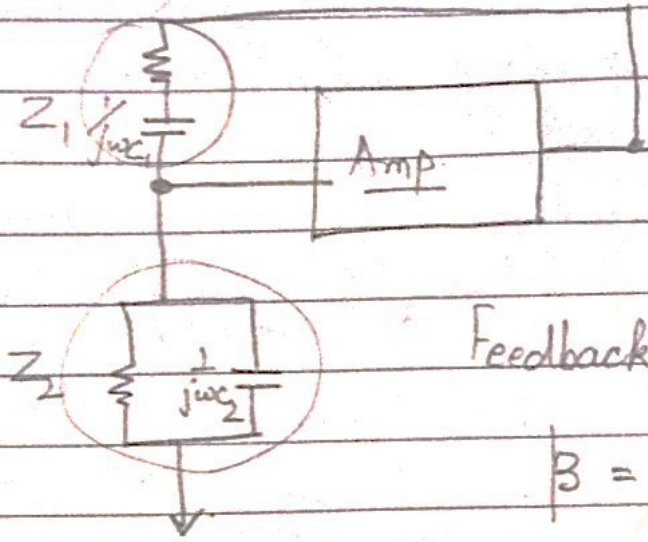
& decide values for R_1 & R_f to get req^d gain. → Done. (detail → later)

* Diff. b/w RC Phase Shift Oscillator & Wein Bridge Oscillator

RC Phase Shift Oscillator	Wein Bridge Oscillator
✓ $f = \frac{1}{2\pi\sqrt{6}RC}$	✓ $f = \frac{1}{2\pi RC}$
– $\lvert A \rvert \geq 29$	✓ $\lvert A \rvert \geq 3$
✓ 180° phase shift in f/b.	– No phase shift in f/b.

Wein Bridge Oscillator, revisited

→ Feedback through RC network



Feedback factor,

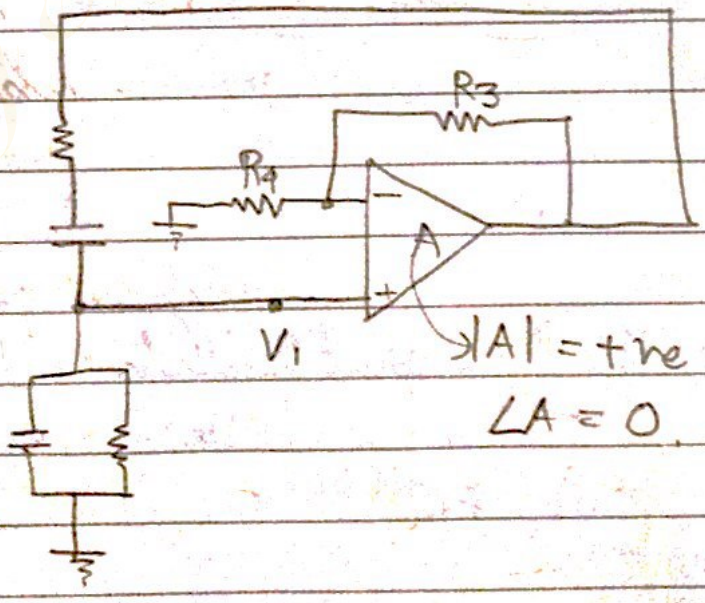
$$\beta = \frac{Z_2}{Z_1 + Z_2}$$

↳ has both magnitude & phase

Part-2 Now, solving to make $\angle A = 0$

(So, gain should a positive real value to get this done)

↳ Log make amp. as "non inverting opamp



Detailed : Designing Wein Bridge Oscillator circuit to have o/p freq of 10 kHz

It difficult to design / manage a capacitor.

So, choose its predefined value

So, let $C = 0.01\ \mu F$ (choosing some intermediate value)

Now, $R = \frac{1}{2\pi fC} = \frac{1}{2\pi \times (10\times10^{3}) \times (0.01\times10^{-6})} = 1.5915\ k\Omega$

$\Rightarrow R = 1.59\ k\Omega$.

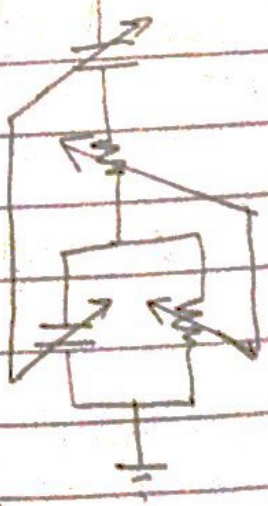
So, choosing a std. value of $1.5\ k\Omega$

Potentiometer

Ganged capacitor

↳ The motion of 2 plates using the spindle changes the capacitance

Idea :



Here, we are using ganged resistors & capacitors, both changing simultaneously

So, $R_1 = R_2$ & $C_1 = C_2$

Now, choose $R_f = 2\ k\Omega$ & $R_1 = 1\ k\Omega$

$A = (1 + \frac{2}{1}) = 3$

∴ ∃ 3 5k resistors stacked in series

IC 555 TIMER

(continued after Square wave & Triangular wave generators)

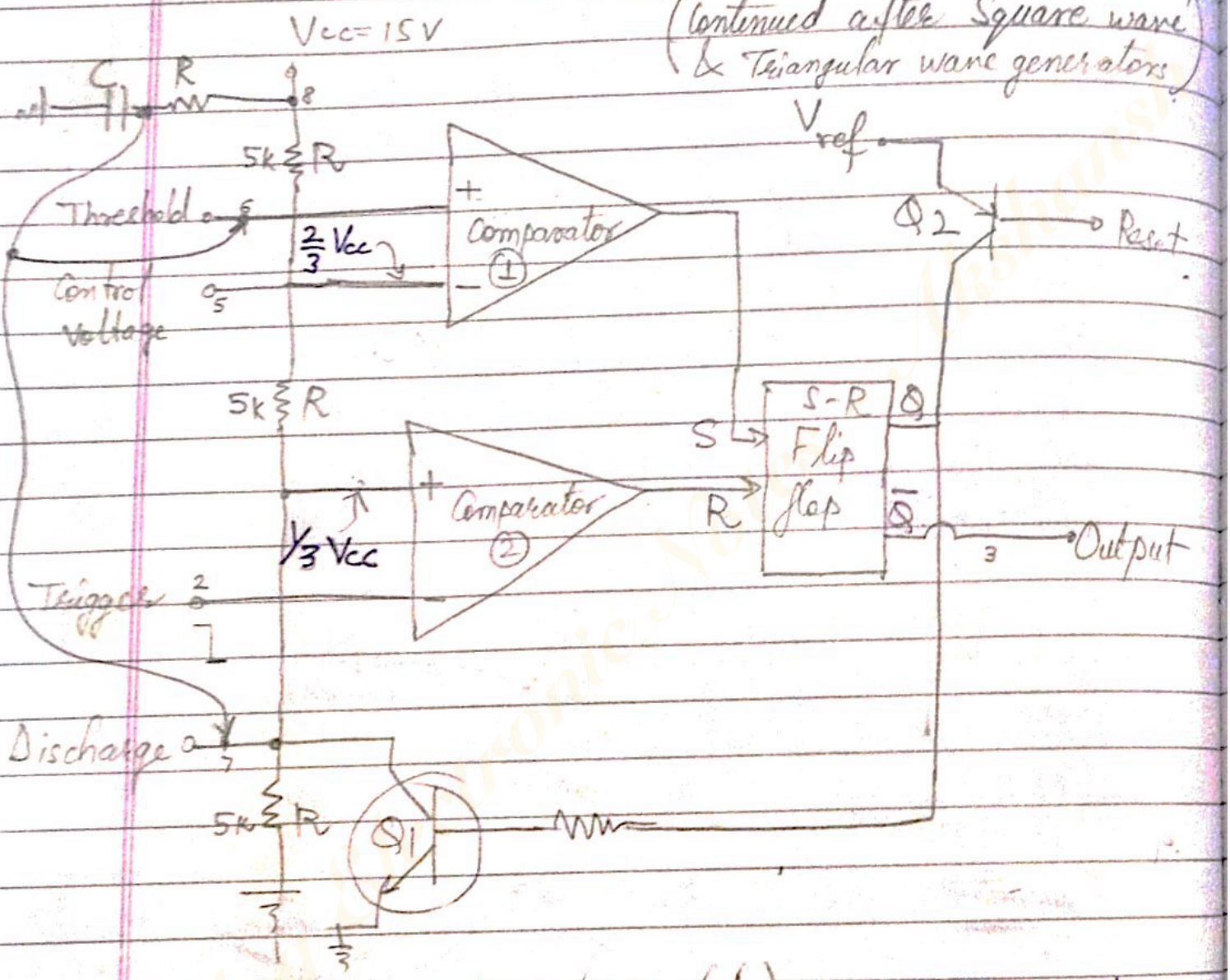
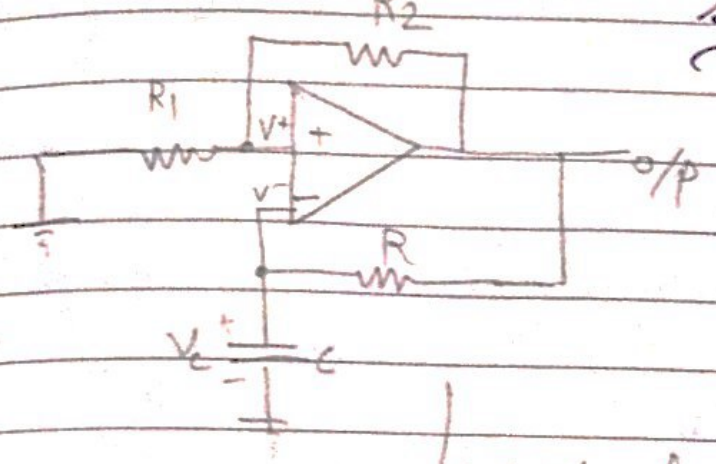


figure (A) : Monostable operation

* Comparators can be used along with capacitors
One comparator notes capacitor charging
Other comparator notes capacitor discharging
The idea is used in Square wave generator

Square Wave Generator



↳ part of o/p is charging the capacitor & at some point, it will reach V_c.

Now,

$$V_+ = \left(\frac{R_1}{R_1+R_2}\right)(V_0)$$

V_0 → can be $+V_{sat}$ or $-V_{sat}$

$\frac{R_1}{R_1+R_2}$ → β.

↳ If $V_0 = V_{sat}$

≃15V ← V_{sat} will charge capacitor & its voltage will increase : $V_c \rightarrow V_{sat}$.

Charging will be done @ time constt

⇒ @ RC

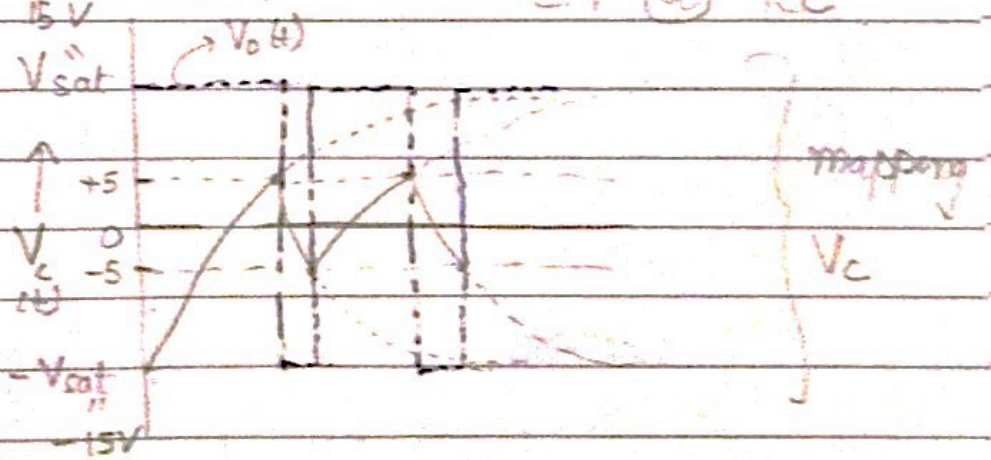
If $V_{sat} = 15V$

$\beta = 1/3$

$\therefore V_{LT} = -5V$

$V_{UT} = +5V$

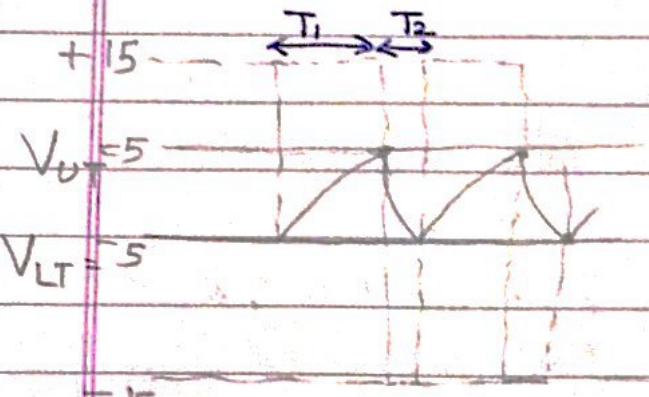
Upper threshold



Starting from -5V, capacitor keeps charging. Now, as capacitor voltage touches 5V, o/p switches to -5V. Hence, βVo also switches from +5 to -5V.

The capacitor now starts to discharge from +5V. Now, as soon as it reaches -5V, o/p switches back to +15. So, $\beta V_o = +5V$. So, charges again.

Clearly, o/p voltage shows a sq wave generation.



Total time = $T_1 + T_2$

freq = $\frac{1}{T_1 + T_2}$ (one cycle)

Note: Charging: V_{LT} to V_{UT}
Discharge: V_{UT} to V_{LT}

Charging: $V_{C(t)} = V_{SAT} - (V_{sat} - V_{LT})e^{-t/RC}$ → (1)

Discharging: $V_{C(t)} = -V_{SAT} - (-V_{SAT} - V_{UT})e^{-t/RC}$ → (2)

↳ eqns to model charging & discharging

In charging, when $V_{C(t)} = V_{UT}$, time = T_1
In discharging, when $V_{C(t)} = V_{LT}$, time = T_2
Note: $V_{UT} = \beta V_{sat}$ & $V_{LT} = -\beta V_{sat}$

From eqn (1),

$$\beta V_{sat} = V_{sat} - (V_{sat} - (-\beta V_{sat}))\, e^{-T_1/RC}$$

$$\Rightarrow \beta V_{sat} = V_{sat} - (V_{sat} + \beta V_{sat})\, e^{-T_1/RC} \rightarrow (3)$$

From eqn (2),

$$-\beta V_{sat} = -V_{sat} - (-V_{sat} - (\beta V_{sat}))\, e^{-T_2/RC}$$

$$\Rightarrow -\beta V_{sat} = -V_{sat} + (+V_{sat} + \beta V_{sat})\, e^{-T_2/RC} \rightarrow (4)$$

eqns (3) & (4) can give T_1, T_2

So, $T = T_1 + T_2$

On solving, we get

$$\boxed{T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)} \rightarrow (5)$$

$$\beta = \frac{R_1}{R_1 + R_2}$$

* Assume $R_2 = 1.164\, R_1$ $\rightarrow$ i.e $\beta = \frac{1}{2.164}$

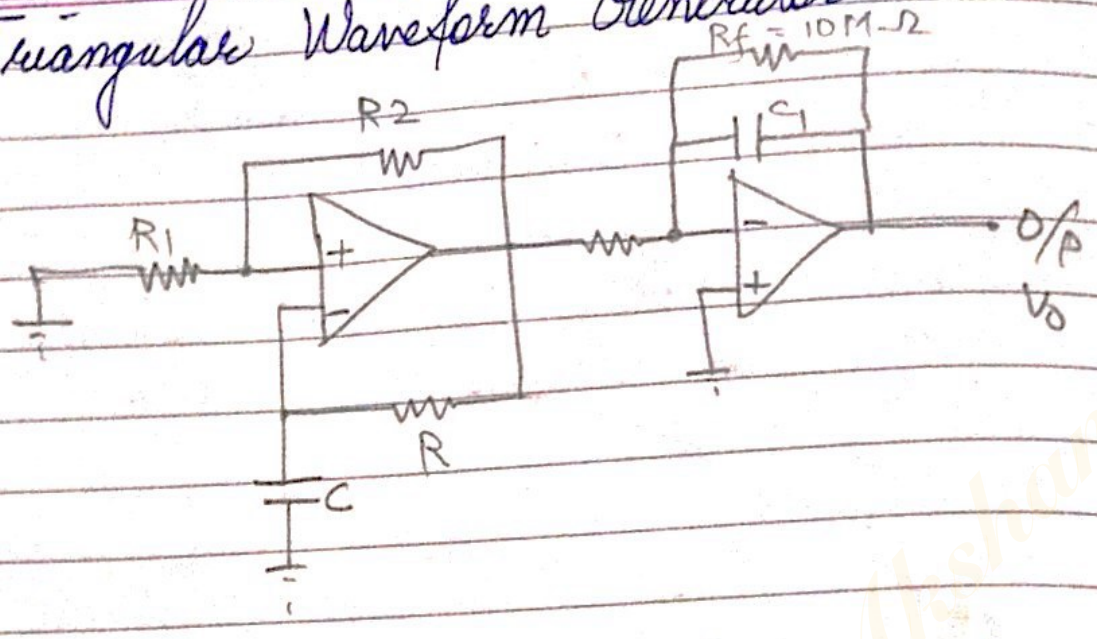
Substitute in eqn (5), we get

$$T = 2RC$$

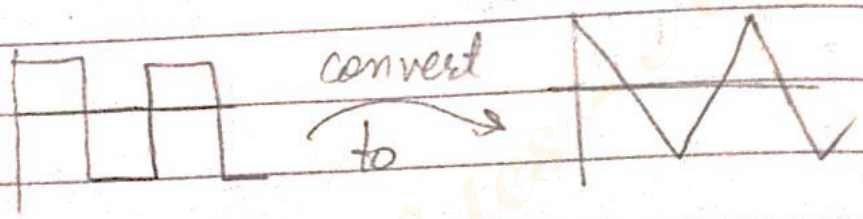
$$\Rightarrow f = \frac{1}{2RC}$$

↳ using this, sq. wave generator can be designed for any freq. (Vary R & instead of C)

✡ Triangular Waveform Generator



Idea :-



Use op-amp integrator

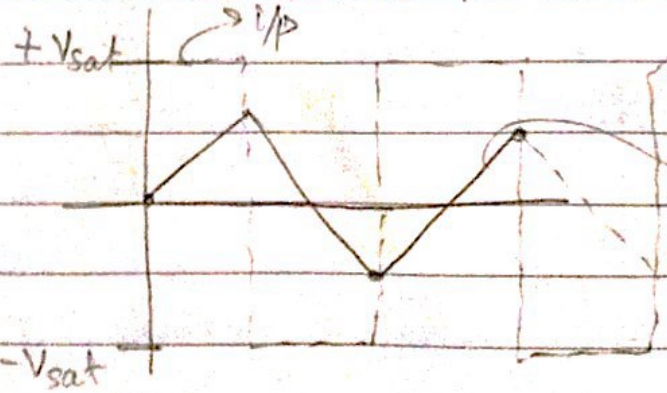
↳ If i/p = constt = V_{sat}

⇒ integrated o/p = $\int V_{sat}\, dt$

$= V_{sat}(t) + c$.

⇒ linearly increasing ramp function

As long as i/p is constt, o/p will continue to rise until it saturates -



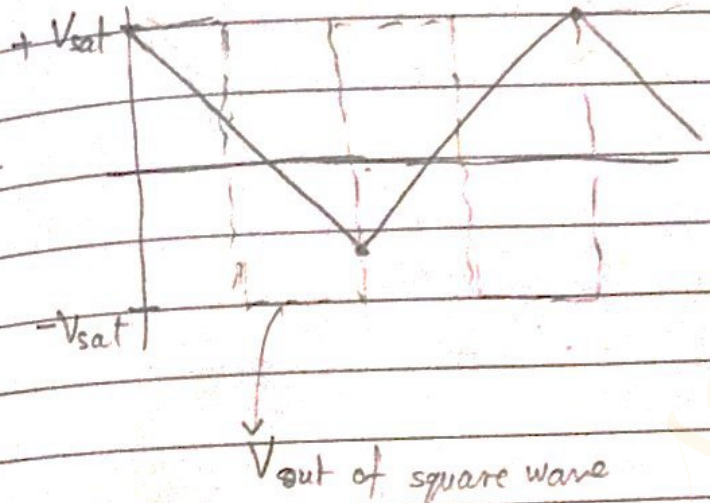
Now, in our circuit on prev. page, (←) we have an INVERTING integrator -

⇒ when sq. wave o/p = +ve

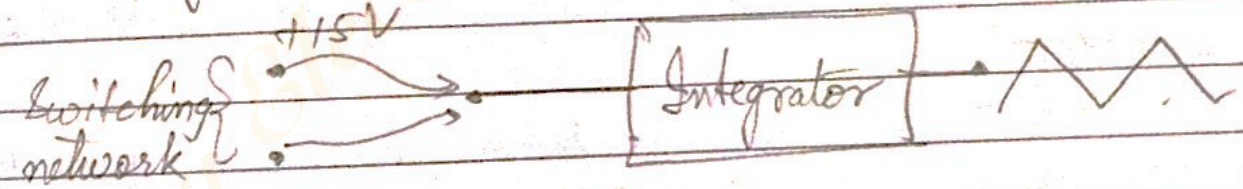
⇓

ramp = -ve slope & vice versa.

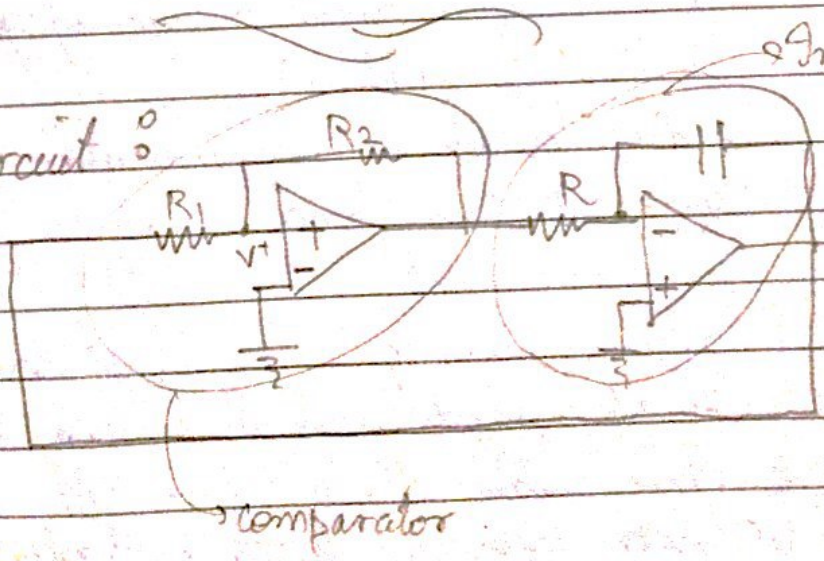
Note : Slope will decide if it touches ± V_{sat} or not.

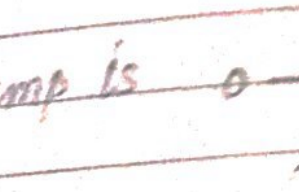


Alter : Instead of using a square wave generator for i/p, take i/p as ± 15V.



Consider circuit :



In the prev. circuit, note: the ramp o/p is being given as i/p to comparator.
So, comparator i/p is changing linearly
So, when ramp is  = crosses zero,
comparator o/p switches from $+V_{sat}$ to $-V_{sat}$
Same happens for -ve ramp.

✡ IC 555 Timer

- ✓ has monostable (pulse) & astable (continuous) multivibrations.
- ✓ can perform DC-DC conversion, waveform generation, temp. measurement, voltage regul".
- ✓ works in a wide range of power supply (+5 V to +18 V).
- ✓ can deliver a considerable amount of power to the load (sinking or sourcing 200 mA of load current)
- ✓ allows timing intervals of several minutes.
- ✓ Its o/p current is high & can drive TTL logic.
- ✓ has high temp. stability.
- ✓ duty cycle of timer is adjustable.

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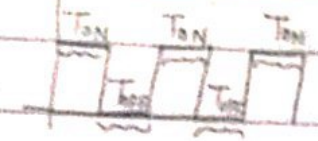
✡ Duty cycle :- $\frac{T_{ON}}{T_{ON}+T_{OFF}} \times 100$

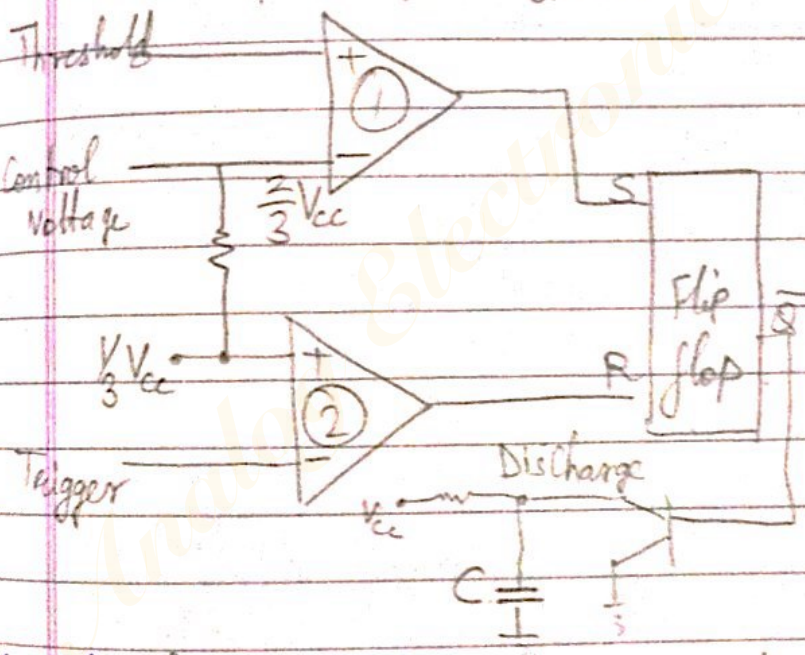


✡ ANALYSIS OF FIGURE(A)

- $\frac{1}{3}$ V_{cc} goes to non-inverting terminal of comparator 2
- $\frac{2}{3}$ V_{cc} goes to inverting terminal of comparator 1

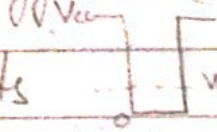
-

S	R	Q	$\bar{Q}$
1	0	1	0
0	1	0	1
0	0	no change	
1	1	Invalid	



Note :

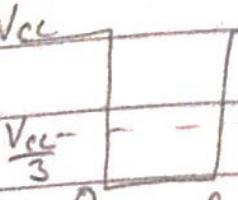
- Comparator o/p is $+V_{sat}$ or $-V_{sat}$
  $+V_{sat} \Rightarrow$ "1"
  $-V_{sat} \Rightarrow$ "0"
- Trigger is (-ve)
  $\Rightarrow$ its



(-ve edge trigger)

Analysis i) (Initial stage) When Trigger = V_{cc}, comparator 2 o/p = $-V_{cc}$ = "0"
$\Rightarrow$ reset = 0 (note : Trigger is not yet applied)
Threshold = V_{cc} gives comparator 1 = $+V_{sat}$ $\Rightarrow$ S = 1 & R = 0, we have Q = 1 & output, $\bar{Q}$ = 0
$\Rightarrow$ base of transistor = (logic 1) $\Rightarrow$ +ve Voltage
Q = 1 goes there $\Rightarrow$ forward bias
So, discharge happens through transistor, charging the capacitor.

Analysis ii) When trigger goes like



When it goes below $\frac{V_{cc}}{3}$, o/p of comparator ② is +Vcc ⇒ reset = 1 ⇒ o/p of SR flip flop = 0 ⇒ Transistor's base part = 0

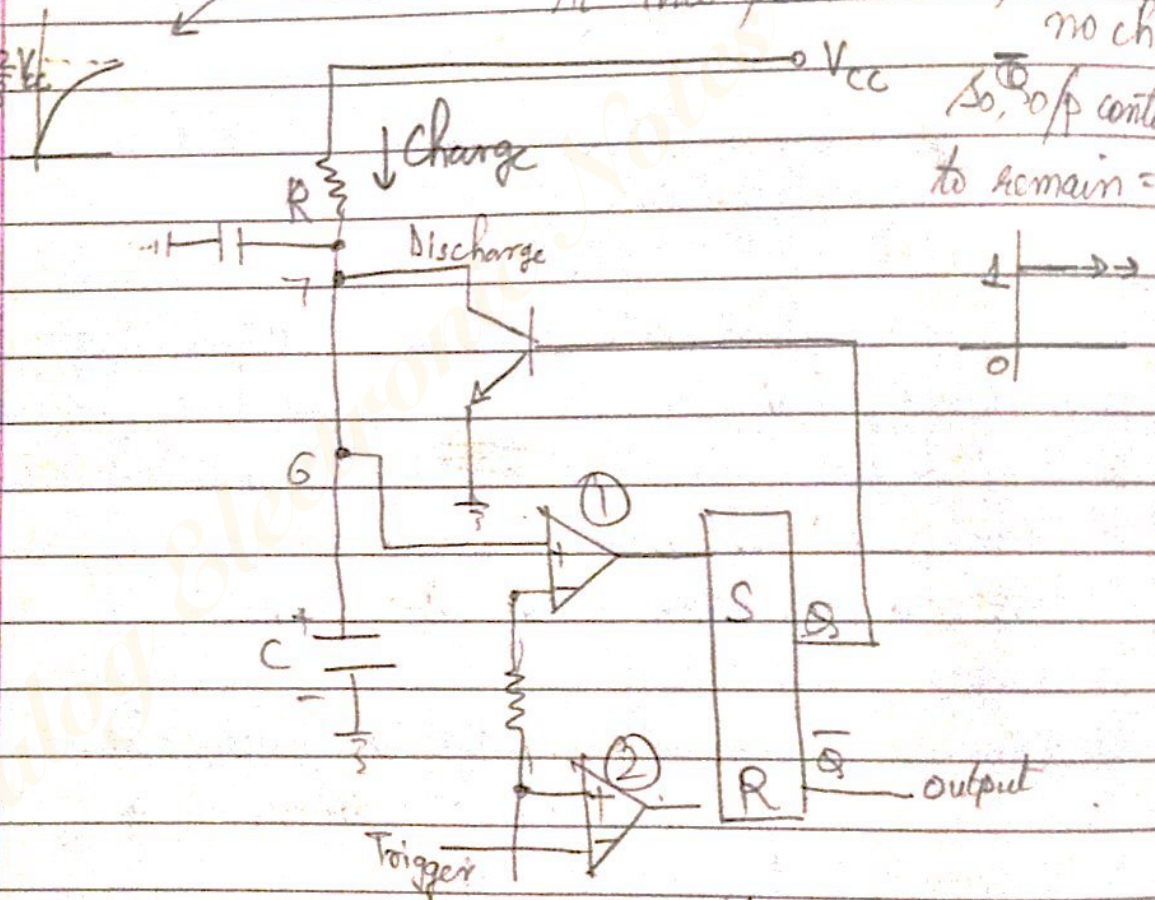
⇒ -ve voltage ⇒ Reverse bias.

⇒ Discharge of transistor stop.

Now, charging of capacitor starts.

At this point S=0, R=0 ⇒ no change

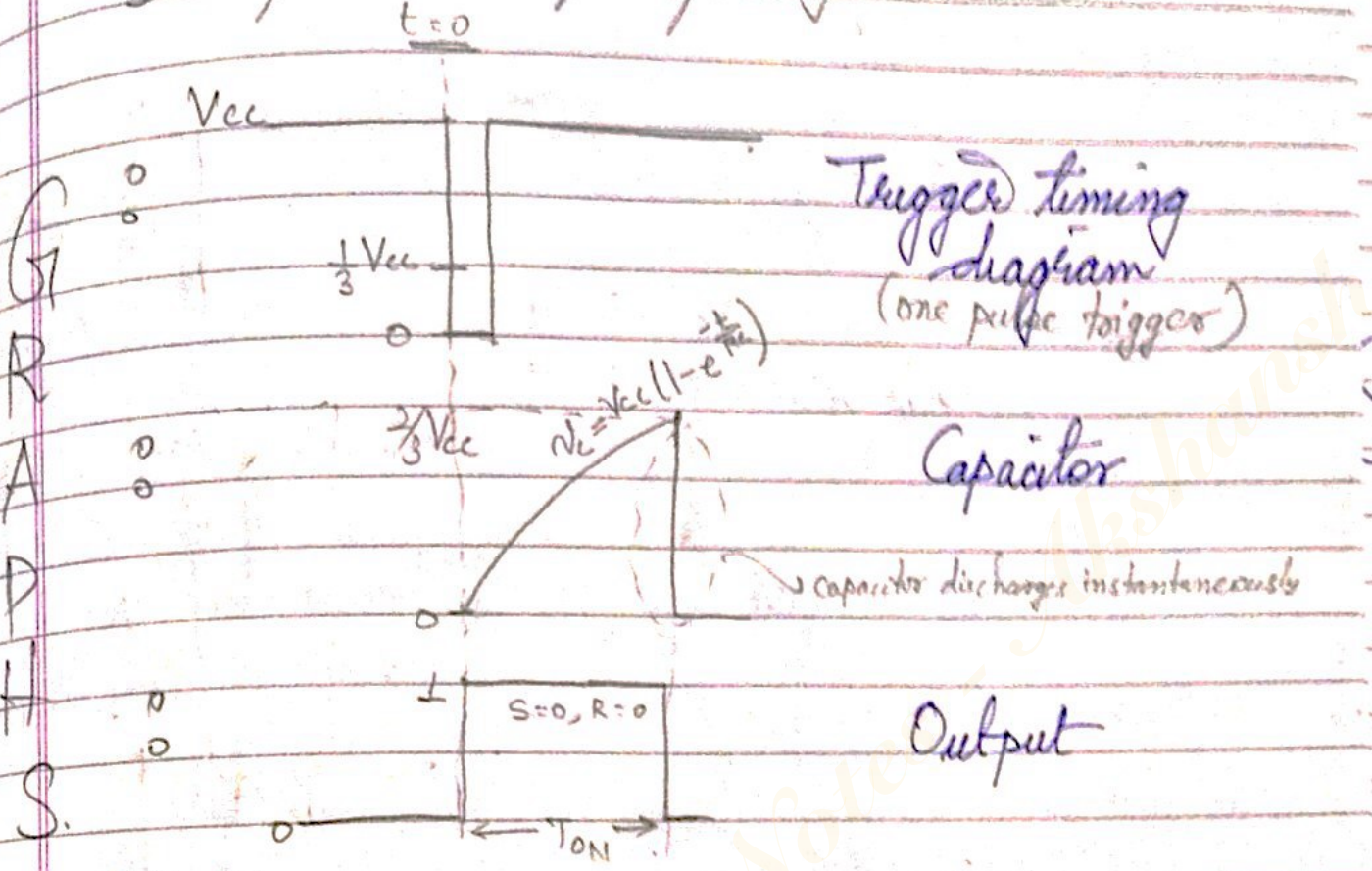
So, o/p continues to remain = 1



Charging continues and tries to go till Vcc. This also compares with 2/3 Vcc of comparator ①. When that is more than $\frac{2V_{cc}}{3}$, o/p of comparator = 1, set = 1

⇒ Discharge activates & o/p becomes zero → (o/p) (capacitor)

This process keeps repeating



GRAPHS.

* Note: In figure (A), ∃ no -ve voltage
So, $+V_{sat} = +V_{cc}$ & $-V_{sat} \doteq 0$.

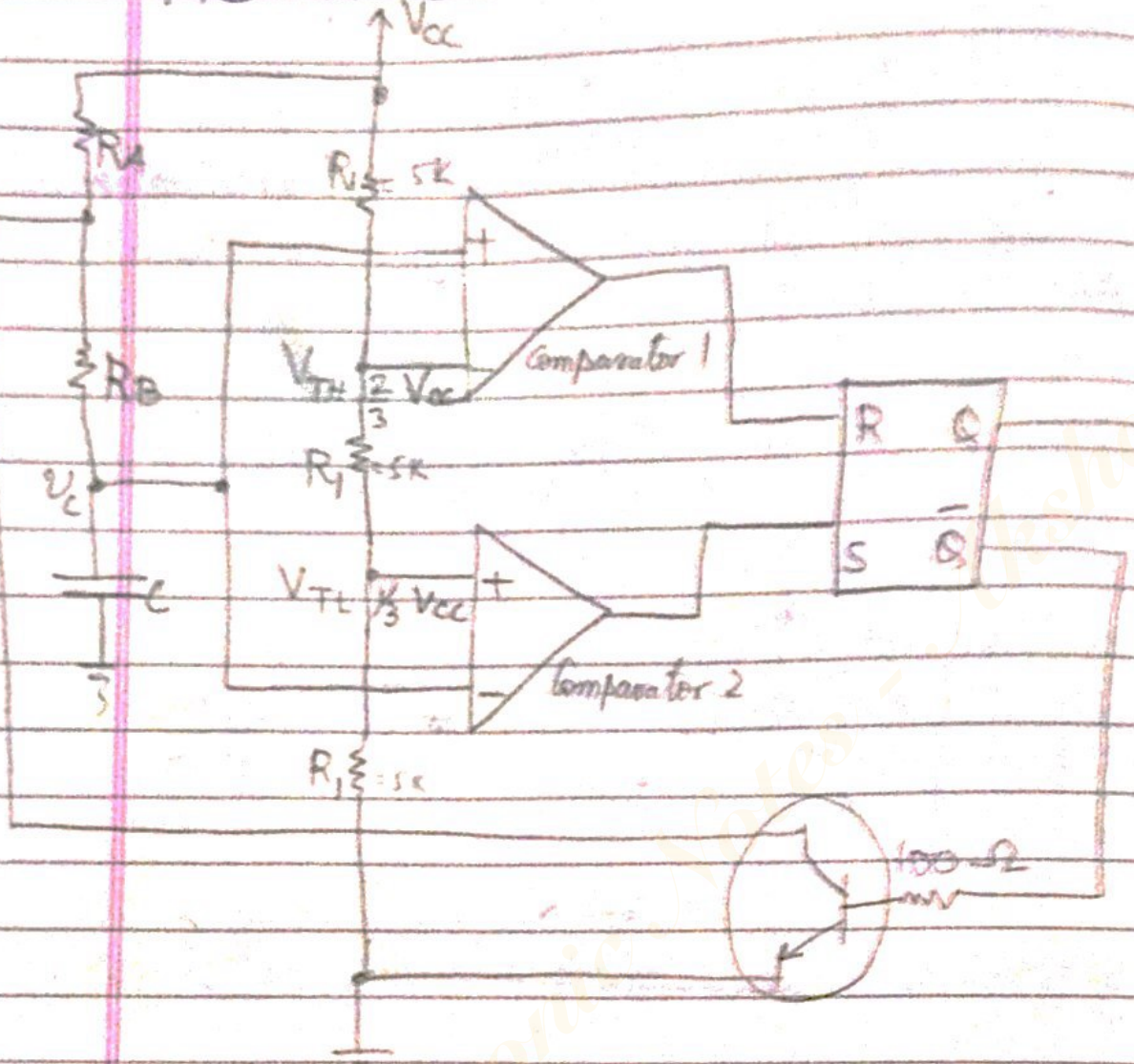
What did we do?
We opened the circuit for sometime & then closed it.
It is the time, the capacitor takes to charge to $\frac{2}{3} V_{cc}$. The charging of capacitor takes place as $V_{cc}(1 - e^{-t/RC})$
So, $\frac{2}{3} V_{cc} = V_{cc}(1 - e^{-t/RC})$

$\Rightarrow T = RC \ln(3)$

$\Rightarrow \boxed{T = 1.1\ RC}$

↳ we can set the time for which circuit is open.

ASTABLE OPERATION



Analysis

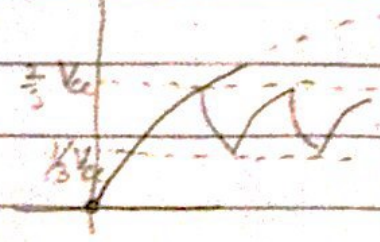
Initially, flip flop is set to 1 (S=1)
(This is done by managing threshold (V_{th}) of comparator 1)

Here,

$Q = V_o = 1\ (V_{cc})$

$\Rightarrow \bar{Q} = 0 \Rightarrow$ Transistor is off

$\therefore$ Capacitor starts to charge with resistance $R_A + R_B$



capacitor charging has 3 stages

V_c : 0 to $1/3 V_{cc}$

$1/3 V_{cc}$ to $2/3 V_{cc}$

$> 2/3\ V_{cc}$ ... continued after next page

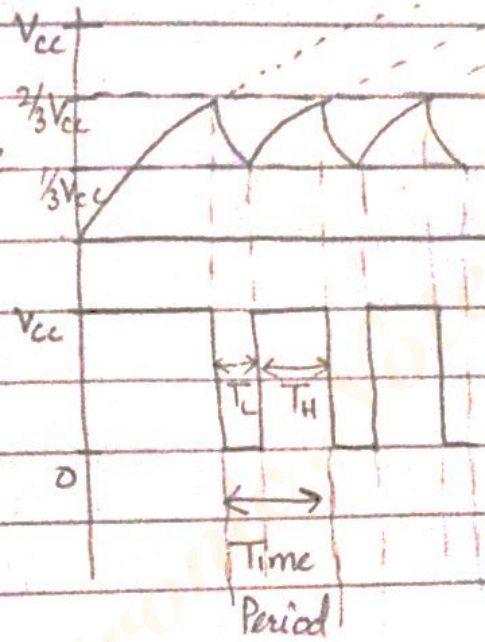
∴ 2 threshold levels : V_{TL} & V_{TH}

V_{TL} → $\frac{1}{3} V_{cc}$ (non inverting terminal of comp. 2)

V_{TH} → $\frac{2}{3} V_{cc}$ (inverting terminal of comp 1)

* Output analyses

Graphs :



Time Period of O/P, $TP = T_L + T_H$

* T_H : during capacitor charges from $\frac{1}{3} V_{cc}$ to $\frac{2}{3} V_{cc}$

Charging, $V_c = V_{cc}\left[1 - e^{-t/(R_A+R_B)C}\right]$

$\frac{1}{3} V_{cc} = V_{cc}\left[1 - e^{-t_1/C(R_A+R_B)}\right]$

$\frac{2}{3} V_{cc} = V_{cc}\left[1 - e^{-t_2/C(R_A+R_B)}\right]$

$T_H = t_2 - t_1$ (done later)

Discharging, $V_c = V_{cc}\left[e^{-t/R_B}\right]$ → gives T_L

V_c → final voltage ($\frac{1}{3} V_{cc}$)

V_{cc} → initial voltage ($\frac{2}{3} V_{cc}$)

Duty Cycle : $\frac{T_H}{T_H + T_L} = \frac{R_A + R_B}{(R_A + R_B) + R_B}$

$= \frac{R_A + R_B}{R_A + 2R_B}$

Analysis of Astable Operation :

Note : o/p = Q

This circuit has two thresholds → V_{TH} & V_{TL}

$V_{TH} = \frac{2}{3} V_{cc}$, $V_{TL} = \frac{1}{2} V_{cc}$

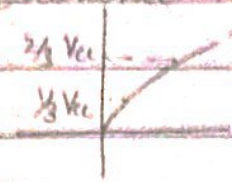
Initially, through some external circuitry, Set of flip flop is made 1 ⇒ S = 1.

(S=1, R=0) ↓ Q=1

As R = 0 ⇒ Q = 1 (= o/p) & $\bar{Q}$ = 0

This $\bar{Q}$ = 0 goes to transistor & deactivates it.

Now, capacitor starts charging from V_{cc}, with resistance $R_A + R_B$. Now, as $V_c > \frac{1}{3} V_{cc}$,



comparator (2) o/p is made 0.

⇒ S = 0 & R = 0 (as before)

(S=0, R=0) ↓ (Q stays 1.)

So, S = 0, R = 0 : Condition for no change.

So, capacitor keeps charging.

As soon as $V_c \geq \frac{2}{3} V_{cc}$, comparator (1) o/p gives 1

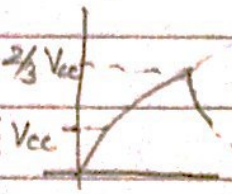
(S=0, R=1) ↓ $\bar{Q}$ = 0, Q = 1

⇒ R = 1. This resets the flip flop.

So, now Q = 0 & $\bar{Q}$ = 1

Now, transistor is activated & discharge of capacitor takes place through R_B.

Now, as soon as $V_c \leq \frac{1}{3} V_{cc}$,



capacitor (2) o/p = 1

(S=1, R=0) ↓ Q=1

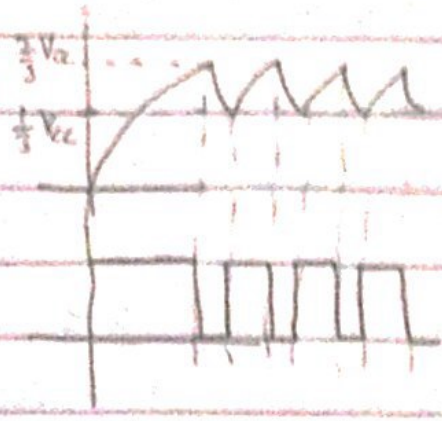
⇒ S = 1. So, Q = 1, $\bar{Q}$ = 0.

So, transistor is deactivated & capacitor starts charging again.

(Also, $V_c < \frac{2}{3} V_{cc}$ So, R becomes 0)

So, like shown before,

Capacitor behaves as



o/p behaves as

Finding ON time (T_H)

$$V_{TH} = V_{TL} + (V_{cc} - V_{TL})\left[1 - e^{-T_H/C(R_A+R_B)}\right]$$

$V_{TH} = \frac{2}{3}V_{cc}$ & $V_{TL} = \frac{1}{3}V_{cc}$

$$\Rightarrow \frac{1}{2} = e^{-T_H/(R_A+R_B)C}$$

$$\Rightarrow e^{T_H/(R_A+R_B)C} = 2$$

$$\Rightarrow T_H = C(R_A+R_B)\ln 2 \quad \rightarrow (1)$$

OFF time (T_L)

$$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\, e^{-T_L/R_BC}$$

$$\Rightarrow T_L = CR_B \ln 2 \quad \rightarrow (2)$$

$$\Rightarrow T = T_L + T_H = C(R_A + 2R_B)\ln 2$$

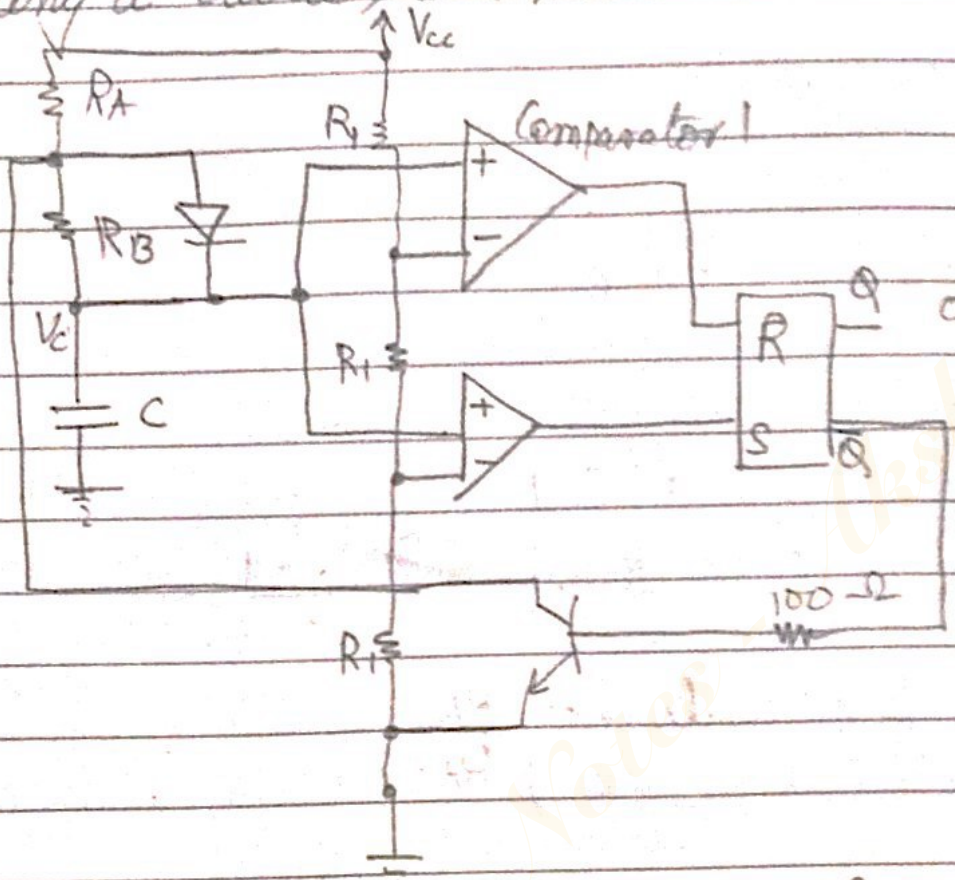
$$\text{Frequency} = \frac{1.443}{C(R_A+2R_B)}$$

$$\text{Duty cycle} = \frac{T_H}{T_H+T_L} = \frac{C(R_A+R_B)\ln 2}{C(R_A+R_B)\ln 2 + CR_B\ln 2} = \frac{R_A+R_B}{R_A+2R_B}$$

↳ Note: Duty cycle $\geq 50\%$ always.

✡ Symmetrical Charging & Discharging

Adding a diode, as shown (Rest circuit is same)



On addition of the diode, note that now the capacitor charging will happen through R_A ONLY (earlier it was $R_A + R_B$)

So, time const = CR_A

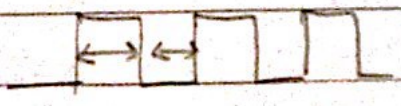
During capacitor discharge, as it can't flow through -ve side of capacitor, So, ∃ no change & discharge happens through R_B (just like before)

So,

$$T_{charging} = R_A C \quad , \quad T_{discharging} = R_B C$$

If $R_A = R_B$. Then, $T_H = T_L$

So, we will get a normal pulse sequence



$$v_c = V_{TL} + (V_{cc} - V_{TL})\left[1 - e^{-t/R_A C}\right]$$

$$\Rightarrow T_H = C(R_A)\ln 2$$

$$v_c = V_{TH}\, e^{-t/C(R_B)}$$

$$\Rightarrow T_L = C(R_B)\ln 2$$

$$\Rightarrow T = C(R_A + R_B)\ln 2$$

$$\Rightarrow \text{Freq} = \frac{1}{T} = \frac{1.443}{C(R_A + R_B)}$$

Duty Cycle :- $\frac{R_A}{R_A + R_B}$

↳ If $R_A = R_B$

⇒ Duty cycle = 50 %

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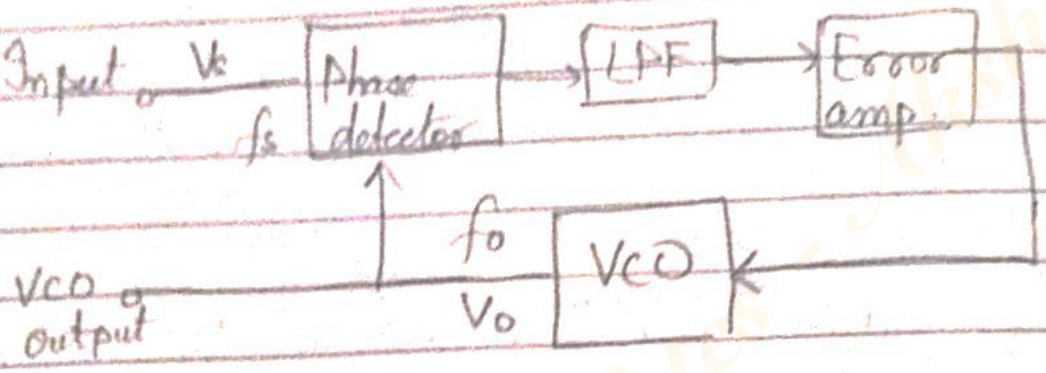
Phase Locked Loop

↳ we want an o/p to lock in phase & freq. w.r.t incoming signal



Consider some freq & phase for i/p. ∃ some sort of feedback, to check for phase difference. This phase detector is usually a freq multiplier.

Mathematically, multiplier o/p =

$$x_m(t) = \underbrace{x_c(t)}_{\text{Input}} \cdot \underbrace{x_f(t)}_{\text{reference}}$$

eg: Let $x_c(t) = A_c \sin(\omega_c t)$

$x_f(t) = A_f \cos(\omega_f t + \phi(t))$

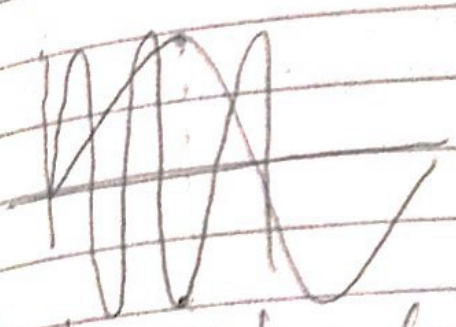
Idea * To analyse $x_c(t)$ & $x_f(t)$:

① Compare freq. first (∵ both cant be compared simultaneously)

∴ if $\omega_1 = \omega_2$

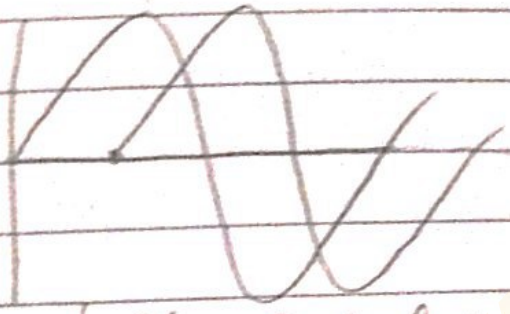
∴ ⇒ o/p has been LOCKED with i/p in terms of freq.

$\omega_1 \neq \omega_2$



↳ can't be analysed

$\omega_1 = \omega_2$



↳ Phase is locked

⇒ If I have maintained same freq, I have LOCKED PHASE.

Now, using analog multiplier (as done before),

$$x_m(t) = A_c \sin(\omega_c t)\, A_f \cos(\omega_f t + \phi(t))$$

↳ we have sin( ) sin( ), cos( ) cos( ) or sin( ) cos( ) terms

So, use trigonometric identities

Now,

$$x_m(t) = \frac{A_c A_f}{2}\left[\sin(\omega_c t - \omega_f t - \phi(t)) + \sin(\omega_c t + \omega_f t + \phi(t))\right]$$

(low freq; high freq)

↳ Now, using a LPF, high freq. component can be removed

Now, o/p, $x_f(t) = \frac{A_c A_f}{2}\sin(\omega_c t - \omega_f t - \phi(t))$

difference freq component

This error is in terms of voltage. This error is amplified (V ↑) in error amplifier

Now, this goes to VCO, it changes its o/p freq to match the frequencies.

Notes: * Phase (or frequency) locking happens ONLY in some range

when i/p is out of freq range

* VCO (Voltage Controlled Oscillator) generates o/p with freq. f_0, even if i/p is absent
* Phase detector is basically an analog multiplier. Phase detector detects phase diff b/w (i/p) & (o/p of VCO).

Now, if $\omega_c \simeq \omega_f$, we get

(ω_c: from i/p, ω_f: from VCO)

$$y(t) = x_f(t) \simeq -\frac{A_c A_f}{2} \sin(-\phi(t))$$

↳ $\phi(t) << 1$

$$\Rightarrow x_f(t) \simeq -\frac{A_c A_f}{2} \phi(t)$$

$\phi(t)$ → Phase difference b/w 2 signals.

↳ This is error voltage $y(t)$

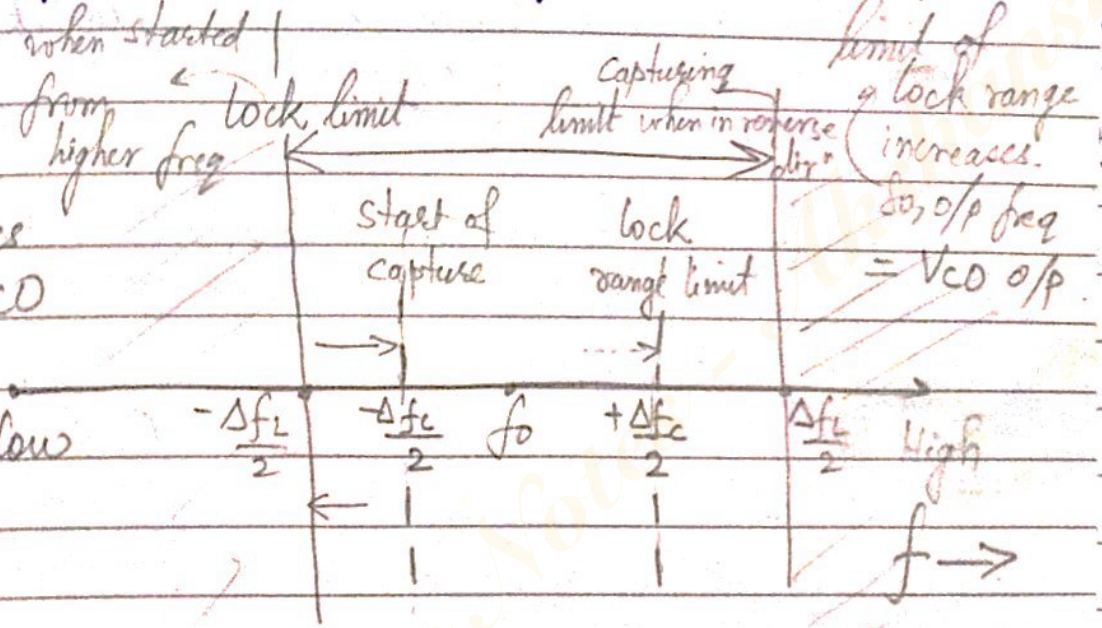
So, freq of VCO is governed by o/p of filter

$$\omega_2(t) = \omega_f + g_v\, y(t)$$

As we say, to lock phase, $y(t) = -A_c A_f \phi(t)/2$

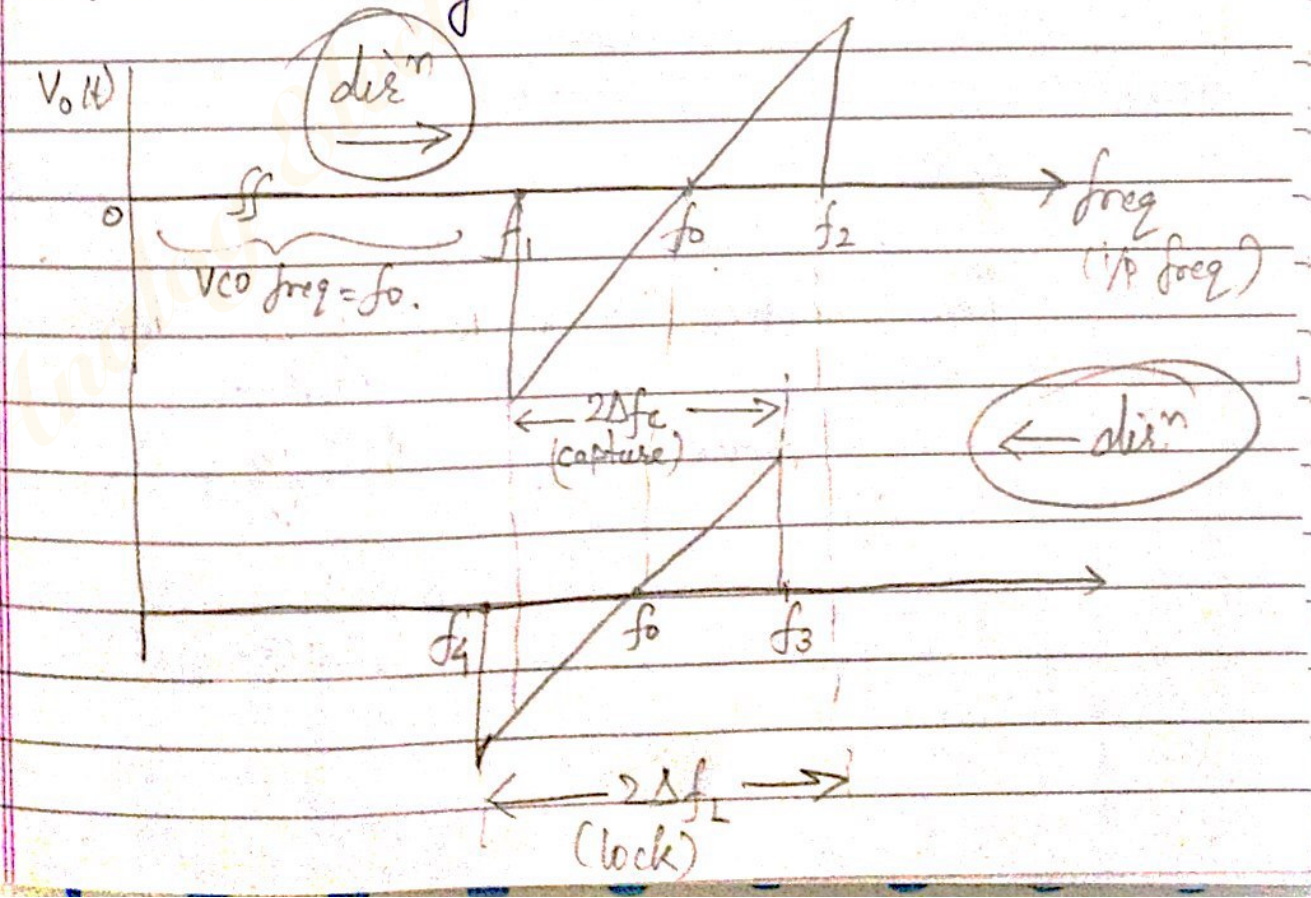
* Lock Range

When PLL is in lock, it can track freq changes in the incoming signal. The range of freq over which the PLL can maintain lock with the incoming signal is called lock range or tracking range of PLL



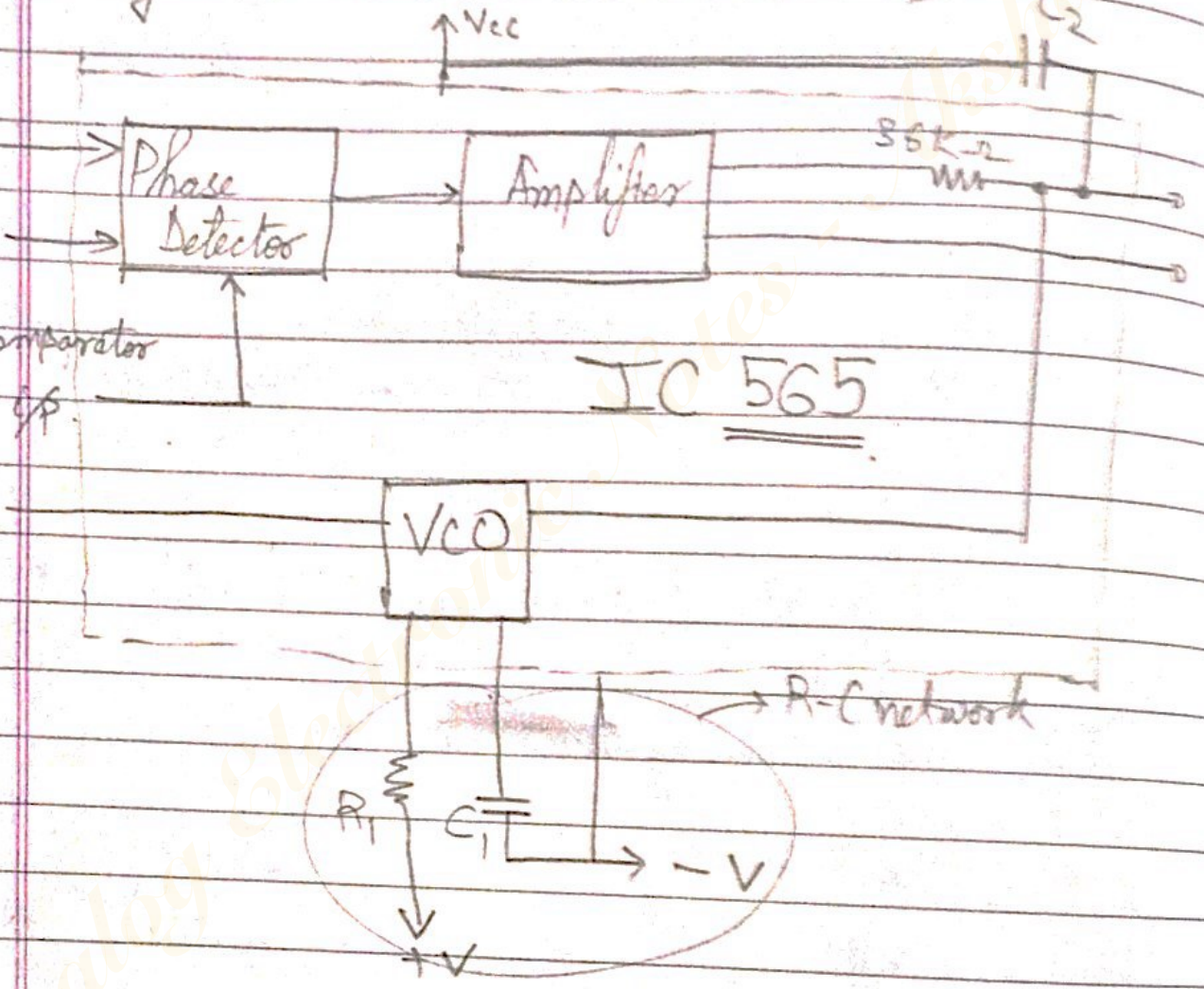
* Pull-in time.

Total time taken by PLL to lock



Basically, as soon as i/p freq comes in the range (in → or ← dir^n), VCO starts to capture & locking oper^n.

* Free running freq (f_o) of VCO can be done by using external connection (R-C network)



Free running freq, $f_o = \frac{1.2}{4R_1C_1}$ Hz.

Also, $\Delta f_L = \pm \frac{8 f_o}{V}$ Hz.

$$\Delta f_C = \pm \left[\frac{f_L}{2\pi (3.6)(10^3) C_2} \right] \text{Hz}$$

eg for PLL circuit, calculate free running freq, lock range & capture range.

Given: $C_2 = 10\mu F$, $R_1 = 10K\Omega$, $C_1 = 0.01\mu F$

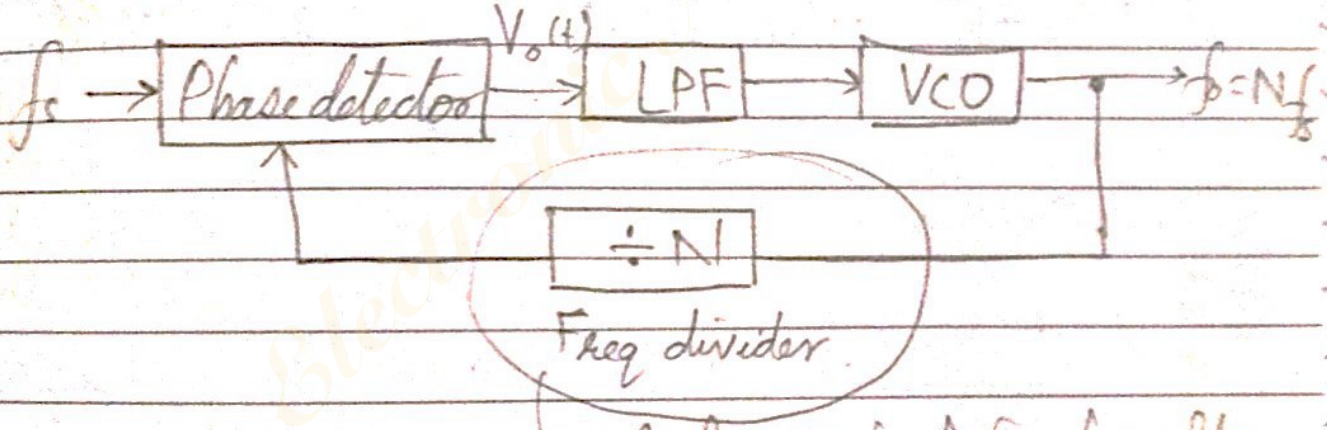
Supply = $\pm 10V$

On calculating using formulas: f_o, Δf_c, Δf_L ✓

---

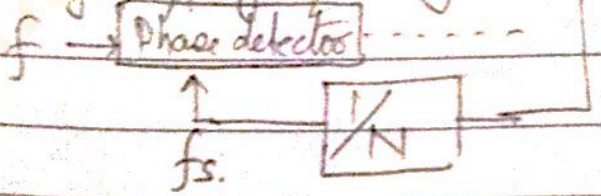
* Application of PLL: Frequency Multiplier

↳ Gives a method of synthesising a freq



→ o/p of VCO is being brought to phase detector

Say, o/p freq = $f_o = Nf_s$.



If $f = f_s$ is maintained, I'll get zero error.

All this happens ONLY within capture range capability of PLL.

eg: Design a PLL, s.t o/p freq = 5x i/p freq.

Given: $f_s = 500$ Hz

$\therefore f_0 = 5 \times 500 = 2.5$ kHz

$f_0 = \frac{1.2}{4R_1C_1}$ Hz

Assume $C_1 = 0.1\ \mu F$

Find R_1, s.t $f_0 = 2.5$ kHz

~

✡

PLL in Digital Signals :-

In this, phase detector is simply an XOR gate that provides the error voltage to LPF.

Consedes 2 signals: x_1

x_2

$x_1 \oplus x_2$: o/p$_1$

x_3

x_4

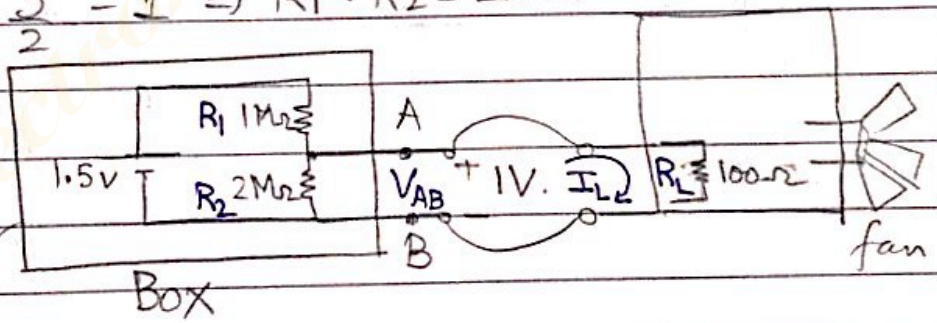
$x_3 \oplus x_4$: o/p$_2$ → o/p

This o/p is phase change error. Pass it through LPF & error detector to VCO.

VOLTAGE REGULATORS

- ✓ no matter whatever load is connected, voltage delivered by source should be constant.
- ✓ Voltage regulⁿ : Voltage change that takes place when load is applied
- ✓ I have std. DC supply of 1.5 V., say. Someone wanted 1 V supply. I want to give him 1 V constantly

$$\left(\frac{R_1}{R_1+R_2}\right)\frac{3}{2} = \frac{1}{2} \Rightarrow R_1 : R_2 = 2:1$$

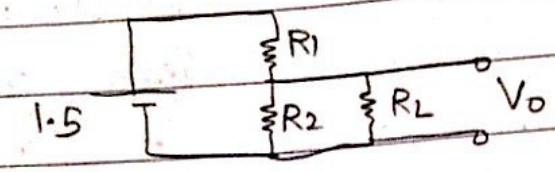


→ If this sys is enclosed in a box & call it 1V power supply, we can drive load

Suppose this 1V is reqd to drive a fan (DC motor) which has $R_{load} = 100\Omega$. Will the fan run after connection is done?

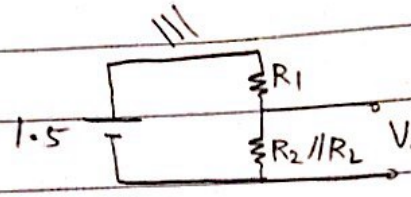
Voltage available across terminals A & B is

$$V_{AB} = \frac{R_2 // R_L}{R_1 + R_2 // R_L} \times 1.5 \simeq \frac{100}{10^6+100} \times 1.5 \simeq 0.$$



$$V_o = \frac{R_2 // R_L}{R_1 + R_2 // R_L} \times 1.5$$

(Potential divider)



Clearly, as $V_{AB} \simeq 0$, fan wont work

Note ①: Loads should have a low value of load resistance so that they can take in more current & operate.

Note ②: We want the power supply to have low o/p resistance. It will be regulated better then.

* % Regulation, $VR = \frac{V_{no\ load} - V_{full\ load}}{V_{full\ load}} \times 100.$

$V_{no\ load} = V_{nL}$ (here, $V_{nL} = 1V$) $= V_{AB}$

$V_{full\ load} \rightarrow V_{fL}$ (comes from the max. current, the supply can deliver to load)

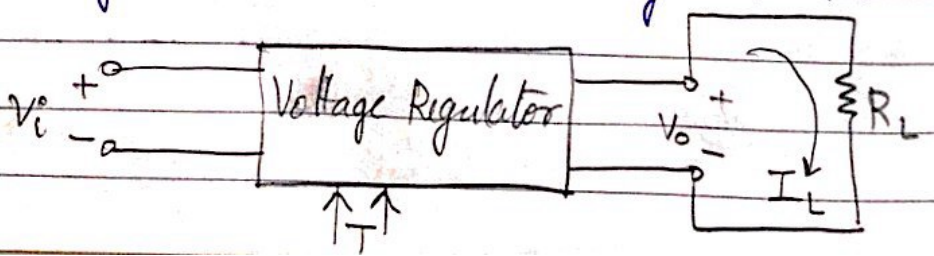
* Let V_o = o/p voltage of supply.

Performance measures:

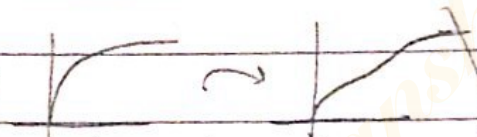
✓ Changes in V_o due to changes in V_i

✓ Changes in V_o due to changes in I_L

✓ Changes in V_o due to changes in T.



* Temp has effect ∵ Voltage regulators have active devices (like transistor, diodes). These devices get heated up. So, their (char. change) So, o/p voltage can change

like 

So, load line changes
So, Q-point changes

• A good voltage regulator should be immune to these changes.

Performance measuring parameters

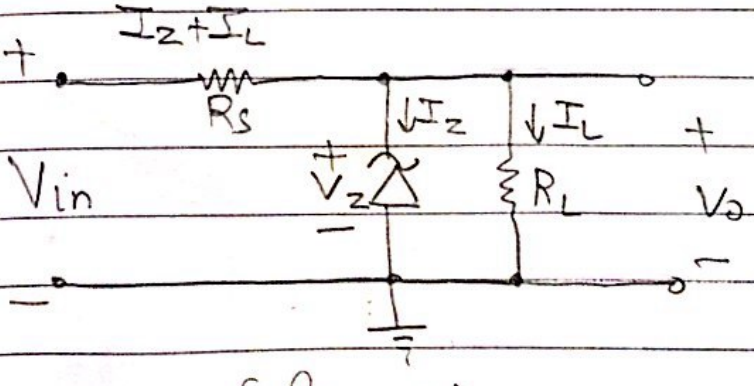
* Stability factor, $S_V = \frac{\Delta V_o}{\Delta V_i}$
  → Ideally, $\Delta V_o = 0$, whatever be ΔV_i

* Output Resistance, $R_o = \frac{\Delta V_o}{\Delta I_L}$

* Temp. Stability factors, $S_T = \frac{\Delta V_o}{\Delta T}$

* VOLTAGE REGULATION CIRCUITS :

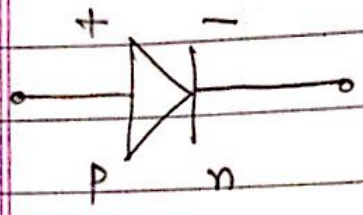
* ZENER REGULATOR :



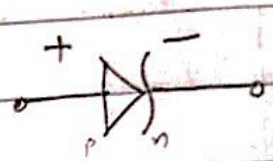
(fig. 1)

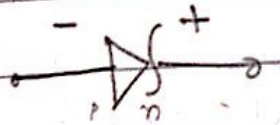
* Note:

Normal diode



Zener diode

FB:  : operating normally

RB:  : operating in breakdown mode

FB : works

RB : doesn't work

* To control the current flow during breakdown, a resistor R_s is placed.

Analysing fig-D (prev page)

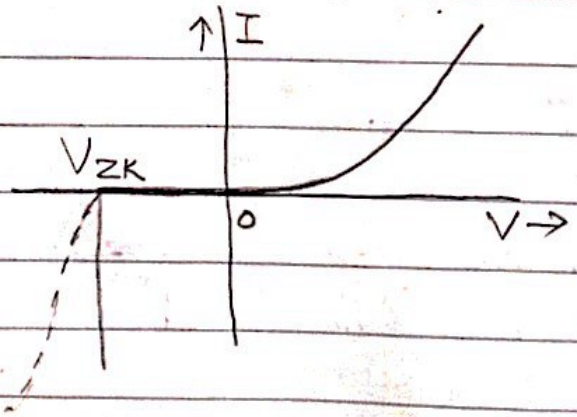
$$V_{in} = R_s(I_L + I_Z) + V_Z$$

$$V_o = V_Z = I_L R_L$$

* Zener regulator is called Shunt regulator.

↳ :: Zener diode is placed in shunt with R_L

Practical char : o/p voltage slighly varies when current across diode is changed.



V_{ZK} is the min. voltage (reverse) req^d to start breakdown process.

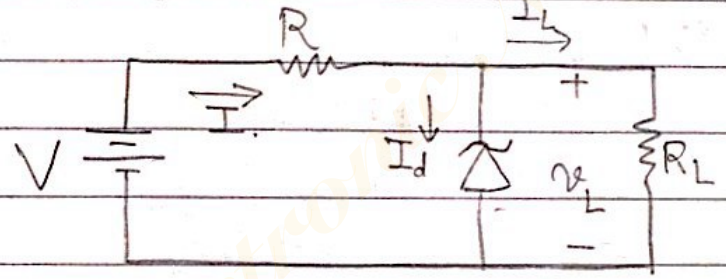
Puffin
Date
Page

- As R_L changes, voltage across R_L remains fixed at $V_Z = V_{ZK}$.
- As load varies, V_{in} should be capable of supplying large current.
- As V_{in} changes, $V_o = V_Z$

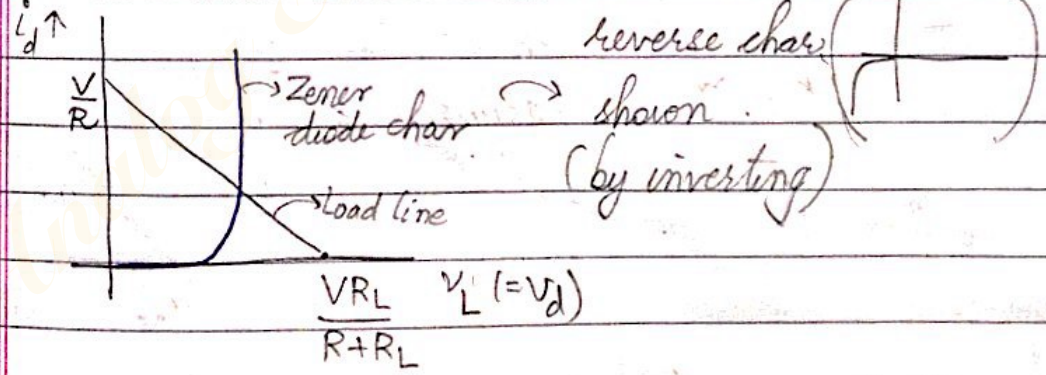
* For non ideal zener:
  Voltage across the diode slightly changes for changing current.

* Seeing Voltage Regulation

Consider the circuit:



Load line characteristics



Operating point is the point when I & V are got across diode normally. (lies on load line)

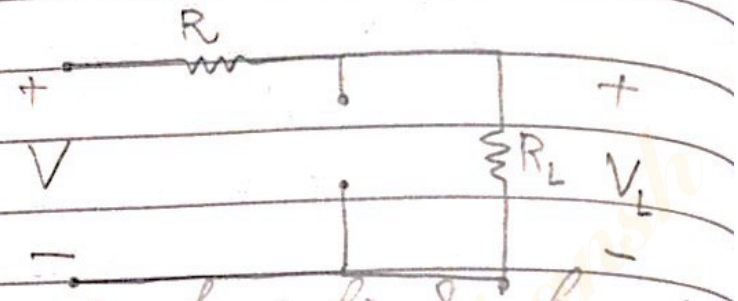
$V = RI + v_L \rightarrow (1)$

↳ when $v_L = 0$, $I = V/R$
↳ when $I = 0$, $V = \frac{VR_L}{R+R_L}$

} (on graph above)

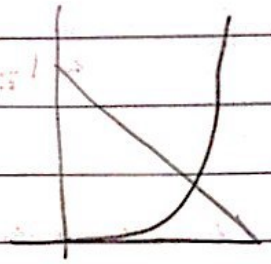
When $I_d = 0$. $\Rightarrow$ current through Zener diode = 0

$\Rightarrow$ Something like :-



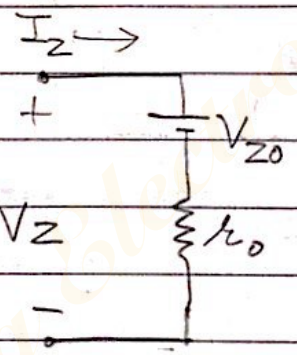
$\Rightarrow V_L = V_o = \left(\frac{R_L}{R+R_L}\right) V$.

* Pt. of intersection b/w load line & char. of Zener diode is called Operating point



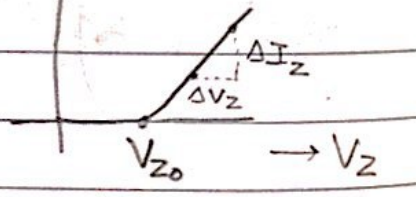
As load line changes, on change of i or v, the Q-point varies

* Zener diode impedance :

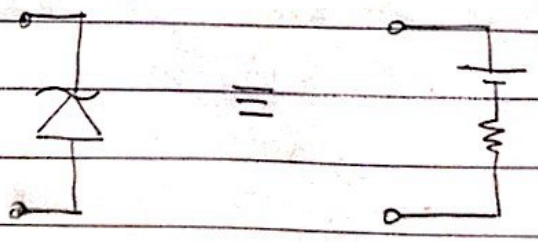


Note :- I want to analyse reverse char. $\left(\begin{array}{c} \nearrow \\ + \end{array}\right)$

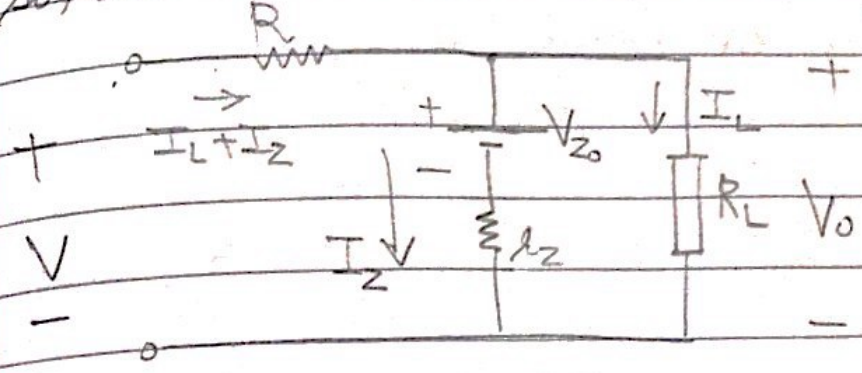
Now, instead of using 3rd quadrant, I invert it to come into 1st quadrant & analyse it



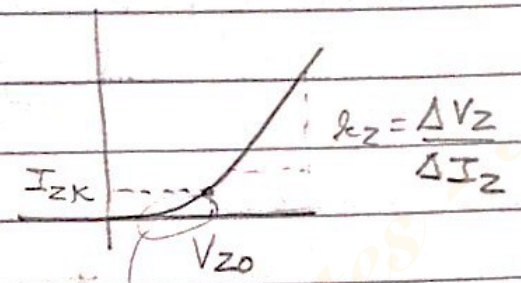
So, on doing that,



So, circuit becomes:



Now, the characteristics are



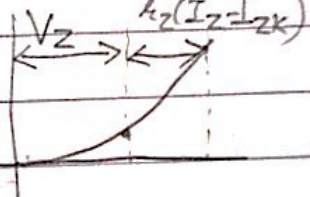
Modelling voltage:
Assuming st line, $r_z = \frac{\Delta V}{\Delta I} = \frac{V_Z - V_{Z0}}{I_Z - I_{ZK}}$

$V_Z = V_{Z0} + r_z(I_Z - I_{ZK})$

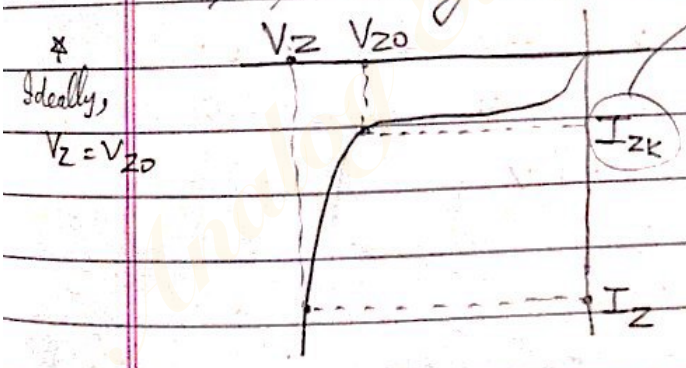
$\rightarrow I_Z > I_{ZK}$

$\rightarrow V_Z > V_{Z0}$

→ I don't want to include the curved portion. (only linear for R_Z)



So, actually, it's:



→ min. current needed to be put across Zener diode to enable Zener action.

Ideally, $V_Z = V_{Z0}$

So, $V_Z = V_{Z0} + r_z(I_Z - I_{ZK})$

$\rightarrow 0$, usually

$\simeq V_{Z0} + r_z I_Z$

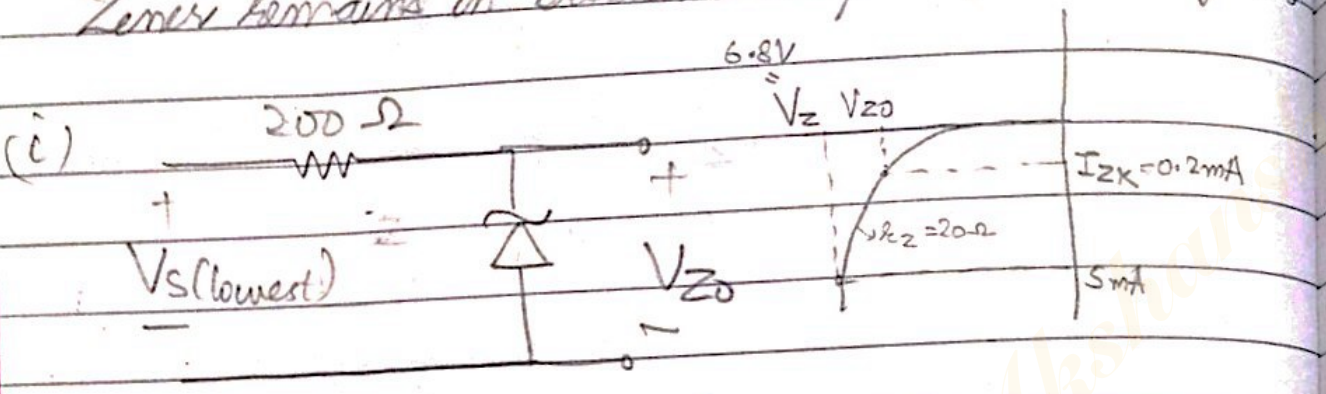
(assumed ∵ practical purpose)

Q. Consider a 6.8V Zener diode, specified at 5mA with $r_z = 20\Omega$ & $I_{ZK} = 0.2$mA is operated in a regulator circuit using 200-Ω resistor.

(i) For no load, what is the lowest supply voltage for

which Zener remains in breakdown opern?

(ii) What is the max. load current for which Zener remains in breakdown opern (Assume supply voltage = 9V)?



Note: Voltage across Zener = lowest = V_{Z0} only when $I_{ZK} = 0.2mA$

& ∵ R_L is not connected, all current goes through diode

KVL:

$$V_{s(lowest)} = (0.2 \times 200) + V_{Z0}$$

We know; $V_Z = V_{Z0} + r_Z(I_Z - I_{ZK})$

$$\Rightarrow V_{Z0} = V_Z - r_Z(I_Z - I_{ZK})$$
$$= 6.8 - 20\left[5\times10^{-3} - 0.2\times10^{-3}\right]$$
$$= 6.7V$$

⇒ for no breakdown,

$$V_{s(lowest)} = \underbrace{(0.2 \times 200)}_{I_{ZK}\ R_S\ mV} + \underbrace{6.7}_{V_{Z0}}$$

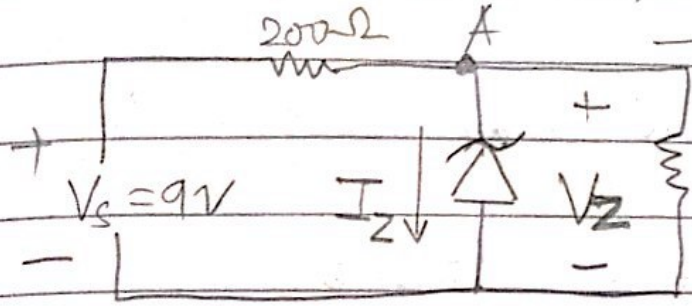
$$\Rightarrow V_{s(min)} = 6.74\ V.$$

⇒ when i/p = 6.74 V, circuit provides o/p of 6.7V & gives current of 0.2 mA.

(ii) Now, $V_S = 9V$

Find max. load current

⇒ ∃ some load. So, circuit is :



• Current & voltage for zener diode $= I_Z, V_Z$

Potential at pt A = V_Z. Change in V_Z is very minimal. So, current across 200Ω is nearly const. This current divides between zener diode & R_L.

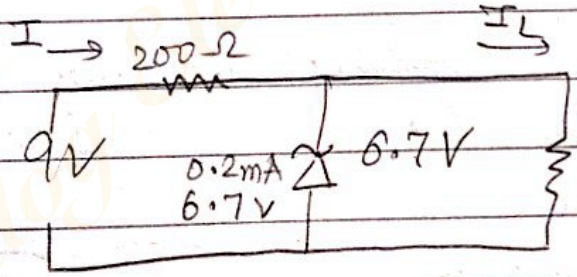
I want to Maximize I_L.

Now, to do that minimize $= I_Z$

We know,

$$\min I_Z = I_{ZK} = 0.2mA$$

So, current across R_L can be found.



So,

$$\frac{(9-6.7)}{200} = I$$

I_2

$$I = (0.2) + I_L$$

$$\Rightarrow I_L = I - 0.2$$

$$\Rightarrow I_L = \left(\frac{2.3}{200}\right) - 0.2$$

$$\Rightarrow I_L = 11.5mA - 0.2mA$$

$$I_L = 11.3mA$$

Also,

$$R_L = \frac{V_Z}{I_L} = \frac{6.7\ V}{11.3\ mA} = \frac{67}{113}\ k\Omega$$

Ans

☆ TEMPERATURE EFFECTS :

Zener diodes are available with breakdown voltage, ranging from 2.4V to 200V.

Temp. coeff. of Zener diode :

$$T.C = \frac{\Delta V_z}{\Delta T} \quad (mV/^\circ C)$$

$$\text{Temp. Stability}_{(S)} = \frac{T.C}{V_z} \times 100\%.$$

* Zener diodes usually have +ve temp coeff. ($T.C|_{\text{Zener diode (RB)}} \simeq 5.5\ mV/^\circ C$.

$T.C|_{\text{Si, not Zener FB diode}} \simeq -2.2\ mV/^\circ C$)

So, if a Zener circuit is taken & temp is changed, Zener voltage changes.

(When large current goes through Zener diode, Temp at junction ↑ ⇒ voltage changes)

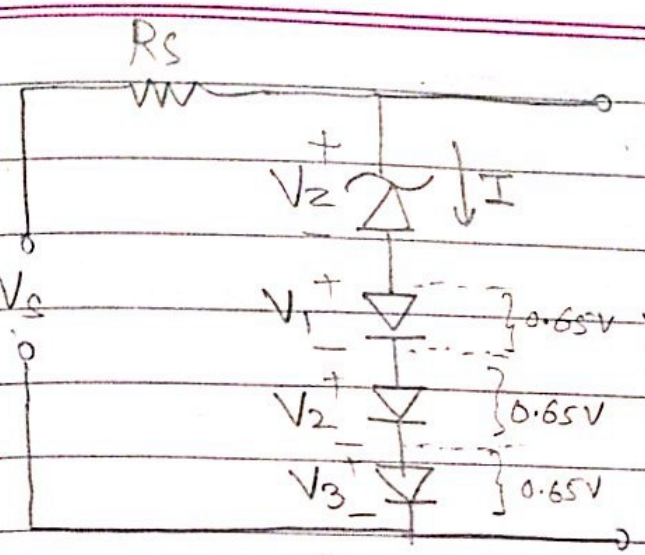
↳ ⇒ Voltage regulation is not happening

How to compensate :

Use temp. compensating circuits :

Use 3 normal diodes alongwith zener diode. So, current flows downward.

(Zener : RB, Normal diodes : FB)



Q Given: $TC\big|_{zener} = +5.5\ mV/°C$.

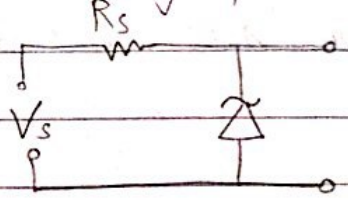
& $TC\big|_{\substack{each\\normal\\diode}} = -2\ mV/°C$.

& $V_Z = 10\ V$ at $25°C$

Forward drop of each diode $= 0.65\ V$

Find:

(i) Temp. Stability of uncompensated zener (i.e, find temp stability of circuit without normal diodes:



$= \frac{(5.5\times10^{-3})}{10} \times 100$

$= 0.055\%$

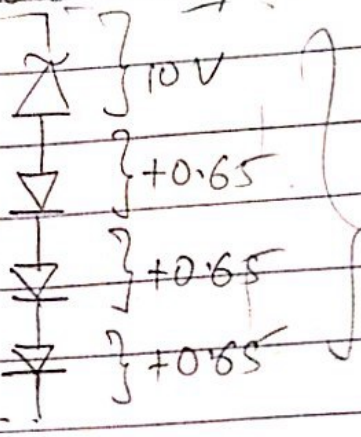
(ii) Breakdown voltage of uncompensated zener at $100°C$.

From $25°C$ to $100°C \Rightarrow 75°$ change

$\Rightarrow 5.5 = \frac{\Delta V_Z}{75} \Rightarrow \Delta V_Z = 5.5 \times 75 \times 10^{-3}$

$\Rightarrow V_Z = 10 + (5.5\times75)\times10^{-3}$.

(iii) Voltage across compensated network at 25°C



(iv) Temp. stability of compensated network

$= (+5.5\ mV/°C) + (-2\ mV/°C) + (-2\ mV/°C) + (-2\ mV/°C)$

Overall $TC = -0.5\ mV/°C$

$\Rightarrow$ Overall Temp. stability $= \frac{\text{Overall TC}}{11.95\ V} \times 100$

$\Rightarrow S_{overall} = \frac{-0.5 \times 10^{-3}}{11.95} \times 100$

$\simeq -0.0041\ \%$

So, without compensation, $S = 0.055\%$

with compensation, $S = -0.004\ \%$

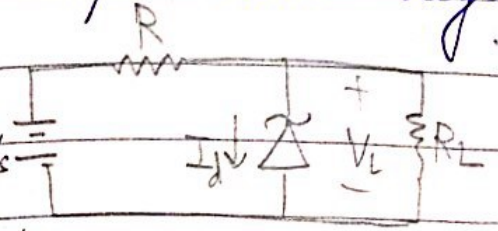
As $S \downarrow \Rightarrow TC \downarrow \Rightarrow \frac{\Delta V_Z}{\Delta T} \downarrow$.

$\Rightarrow$ For any change in temp, $\exists$ very small change in V_Z

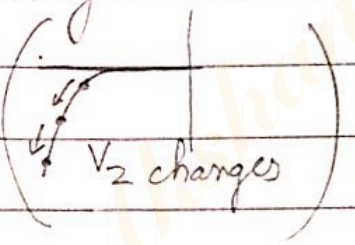
So, Zener voltage doesn't change on temp. change

CONSTANT CURRENT ZENER REFERENCE:

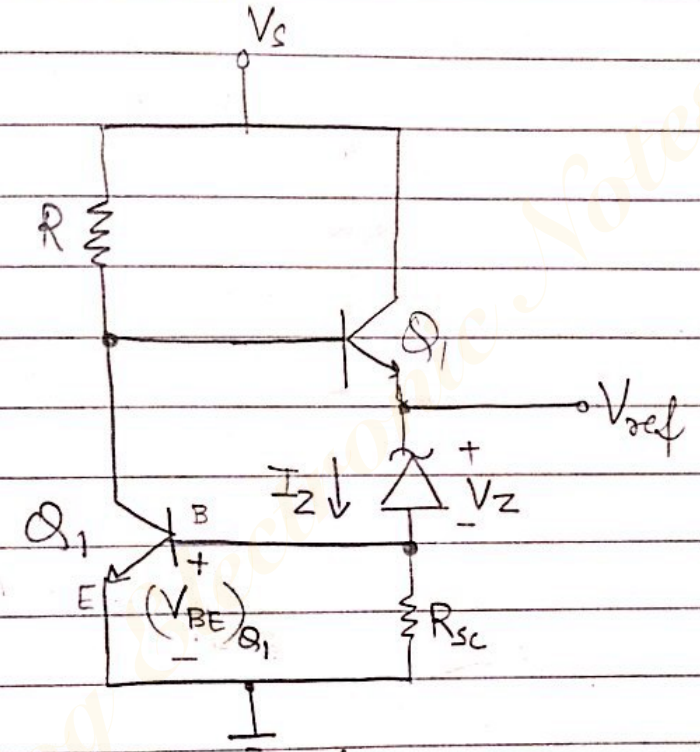
In simple zener & regular had some problems.



When $V_s \uparrow$, $I \uparrow \Rightarrow I_z \uparrow$
&, zener voltage need not remain constt.



Improved circuit:

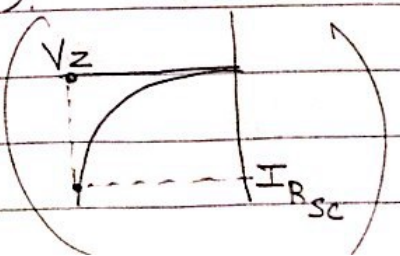


When circuit is active, V_{BE} can be maintained at 0.7V. (Q_1 is // to R_{sc}).

$$\text{So, } I_{R_{sc}} = \frac{V_{BE_{Q_1}}}{R_{sc}} \simeq \frac{0.7}{R_{sc}\ (\text{fixed})}$$

Any current flowing through V_z will also go through R_{sc} ($\because I_b \simeq 0$).

$$\Rightarrow I_{R_{sc}} \simeq I_z$$



So, $V_{REF} = V_Z + V_{BE_{Q1}}$

$V_{BE_{Q1}}$ almost constt

$\Rightarrow$ V_Z almost constt.

$\Rightarrow$ V_{REF} → constt (even if V_s changes)

$\Rightarrow V_{REF} = (V_{Z0} + I_Z r_Z) + V_{BE_{Q1}}$

I_Z : current flowing through zener $= \frac{V_{BE_{Q1}}}{R_{SC}}$

r_Z : Slope of zener curve

$$\Rightarrow \boxed{V_{REF} = V_{Z0} + V_{BE_{Q1}}\left(1 + \frac{r_Z}{R_{SC}}\right)}$$

→ no term depends on V_s

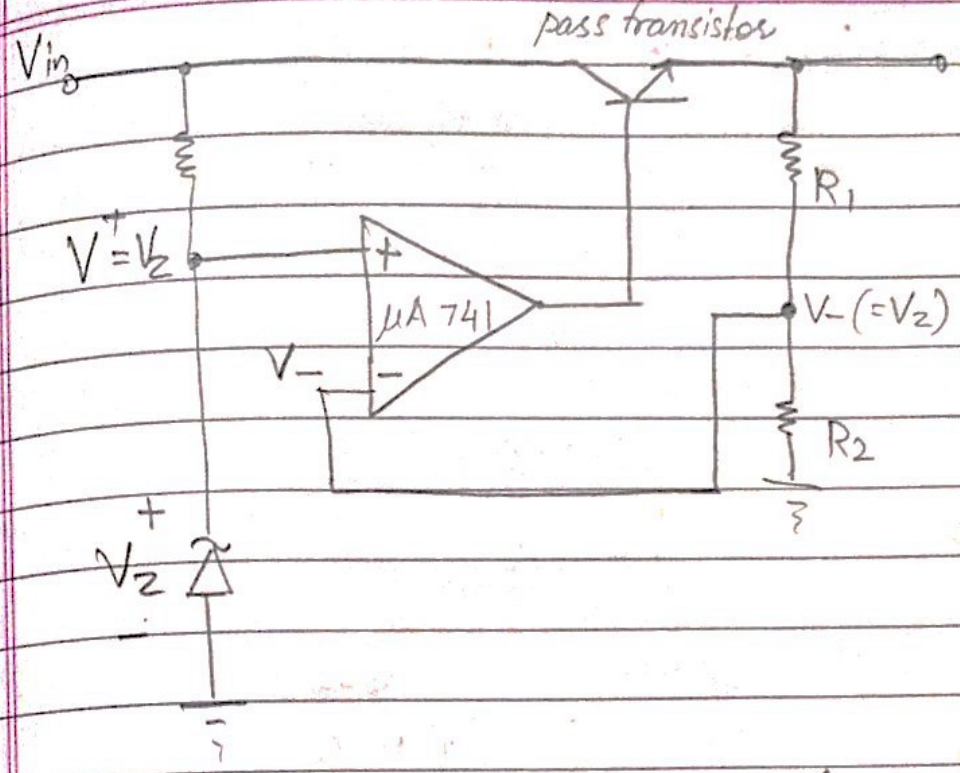
§ SERIES VOLTAGE REGULATOR.

A pass transistor : allowing current going from source to load.

As ∃ -ve feedback ∴ $V_+ = V_-$.

So, $V_+ = V_Z = V_-$.

Now, $V_- = \left(\frac{R_2}{R_1+R_2}\right) V_o \Rightarrow V_Z = \left(\frac{R_2}{R_1+R_2}\right) V_o$.



For V_o to be constant V_Z should be constant

(V_Z | I_{Z_1}, I_{Z_2} $\Rightarrow$ As $V_Z = V_{Z0} + r_Z(I_Z - I_{ZK})$ For $V_Z = V_{Z0}$, $r_Z = 0$)

one drawback $\rightarrow$ non ideal } not possible at all times. So, for a small range, V_o can be taken constant. (i/p fluctuation can be very large)

* Advantage : By adjusting R_1 & R_2, we can make $V_o >> V_Z$. So, value of V_o can be set

eg Design a series voltage regulator using op-amp & 6V-Zener to maintain o/p of 18V (regulated). Assume unregulated i/p voltage (V_{in}) varies b/w 20V & 30V.

Another constraint : $I_{Z\,min} = 20\,mA$ to keep Zener in breakdown.

From prev. fig, $V_Z = 6V$

$V_0 = 18\ V$

$V_{in} \in [20, 30\ V]$

$I_Z = 20\ mA$

① $V_0 = \left(1 + \frac{R_1}{R_2}\right) V_Z$

$\Rightarrow 18 = \left(1 + \frac{R_1}{R_2}\right) 6$

$\Rightarrow R_1 = 2R_2$

↳ let $R_1 = 20\ k\Omega$

$\Rightarrow R_2 = 10\ k\Omega$

Current through R_3 has to flow through zener (if op-amp is ideal). As $I_Z \geq 20\ mA$ (given)

So, min. current going through R_3 should also be 20 mA

Now, $I_{R3} = \frac{V_{in} - V_Z}{R_3} \geq 20\ mA$

$\Rightarrow \frac{20 - 6}{R_3} \geq 20\ mA$

& $\frac{30 - 6}{R_3} \geq 20\ mA$

} ∵ V_{in} varies from 20 - 30.

$\Rightarrow R_3 \leq \frac{14}{20}\ k\Omega$ & $R_3 \leq \frac{24}{20}\ k\Omega$

$\Rightarrow R_3 \leq \frac{7}{10}\ k\Omega \Rightarrow R_3 \leq 0.7\ k\Omega$

(Choosing $R_3 = 700\ \Omega$ gives Zener JUST at breakdown.

Any value $< 700\ \Omega$ is better)

In constant current zener reference, we got $V_o = V_Z + 0.7$
But, in series voltage regulator, $V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z$. So, any value can be set.

Disadvantage: See the o/p area.

$V_o = 18V$.

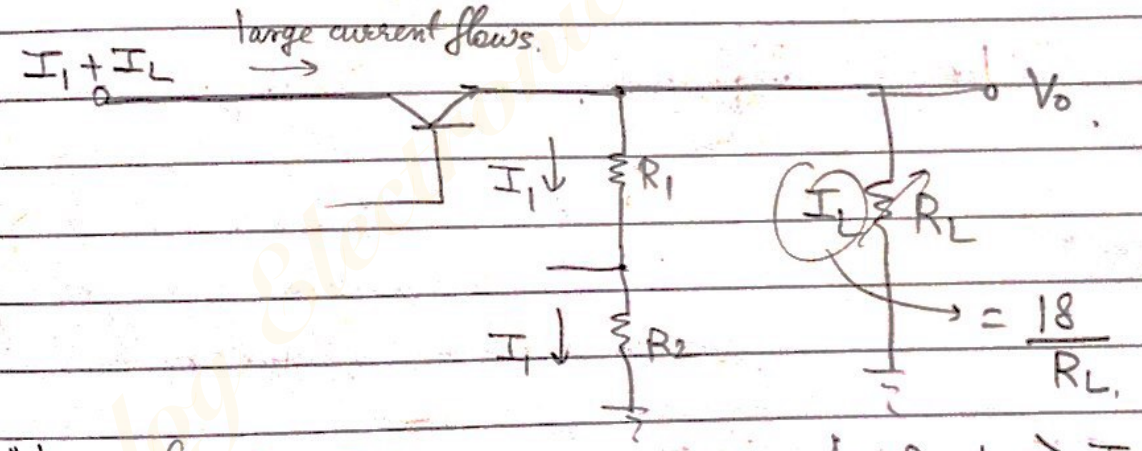
$R_1 + R_2 = 30k\Omega$.

So, current through $R_1 - R_2$ path, $I_{(R_1, R_2)} = \frac{18}{30k\Omega}$

$= 0.6\,mA$.

very small value.

This circuit is a regulator, a supplies of a constt voltage. But, as it cannot supply a very large current, it wont be able to drive a load.



As $R_L \downarrow \Rightarrow I_L \uparrow$.
This excess current requirement is supplied from V_{in}, through transistor. The transistor gets loaded.

Now, for transistor,

lower dissipⁿ ← $P_D = V_{CE} \times I_C$

$P_D = (V_{in} - V_o) \times I_C$

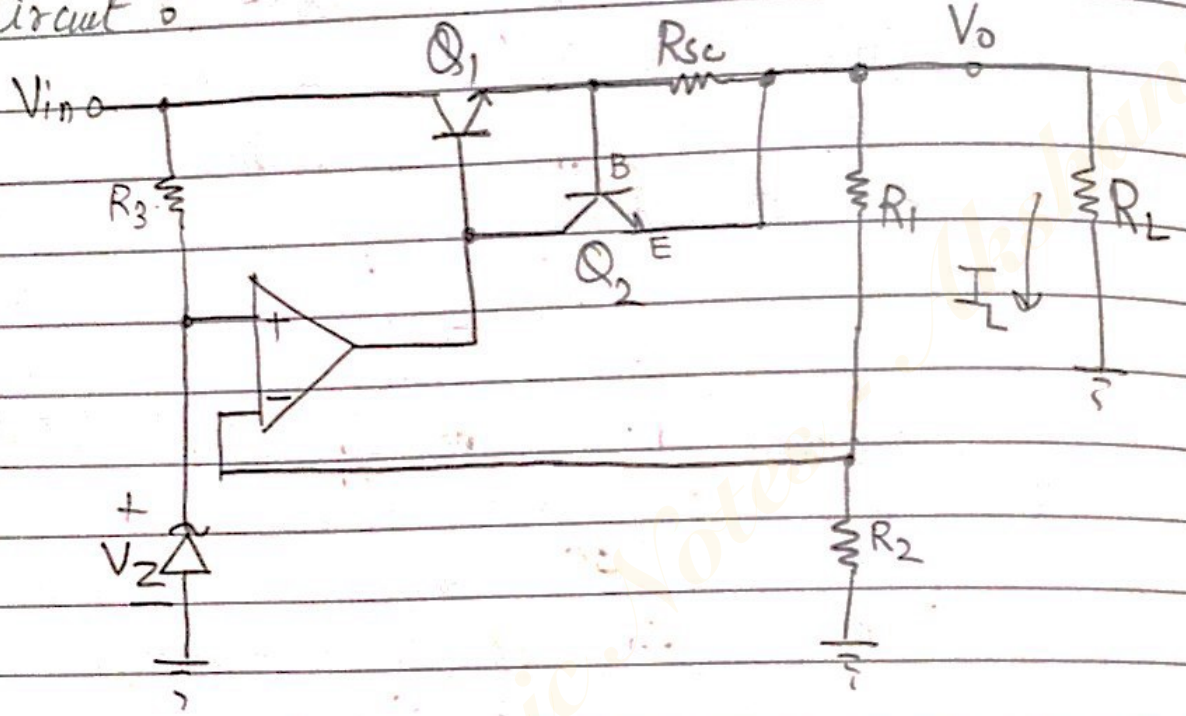
large power dissipⁿ on heat transistor.

Remedy: Limit the amount of current (I_L). This is done by current limiting circuit (PTO)

• Current Limiting Circuits.

To protect Q_1 from excessive power dissipation, add Q_2 in the previous circuit

Circuit :



Potential diff. across $R_{sc} = 0.7$ ($V_{BE_{Q_2}} = 0.7$)

$\Rightarrow I_{R_{sc}} \approx \frac{0.7}{R_{sc}}$.

As $I_{B_{Q_2}} \simeq 0$ (base current $\to 0$)

So, any current flowing through R_{sc} comes from $I_{E_{Q_1}}$

So, $I_{E_{Q_1}} \simeq I_{R_{sc}}$ (∀ practical purposes)

So, current coming out of $Q_1 = \frac{0.7}{R_{sc}}$

Note : R_{sc} is in our hands. So, by apt. choice of R_{sc}, we can limit the current through pass transistor, Q_1.

Now, when load is connected (R_L), it starts drawing current from circuit.

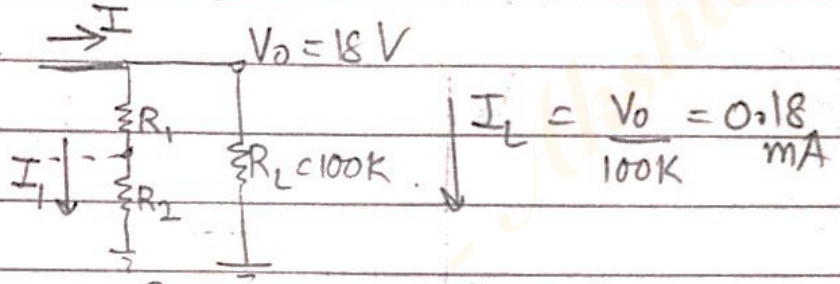
If R_L is small, ∃ no problem, as the current coming is small.

If R_L is large:

We know: $V_o = V_Z\left[1 + \frac{R_1}{R_2}\right]$ ($V_Z \to 6$, $R_1 \to 20k\Omega$, $R_2 \to 10k\Omega$)

$\Rightarrow V_o = 18\,V$

Say $R_L = 100k\Omega$



Some current was already going through $R_1 + R_2$

$I_1 = I_{R_1 \& R_2} = \frac{18}{30} = 0.6\,mA$

$I = I_1 + I_L$

$\Rightarrow I = 0.6 + 0.18 = 0.78\,mA$

If I adjust R_{sc} s.t $I = (1\,A)$. So, it can easily supply current to both resistors

($V_{BE_{Q_2}}$ is adjusting on its own)

If we start decreasing R_L. So, current requirement is increasing. ∃ some point when total current requirement becomes larger than 1 A (which can be supplied through R_L)

(Note $I_1 << I_L$. So, can be ignored)

At this stage, $V_o = V_Z\left(1 + \frac{R_1}{R_2}\right) = 18$

& $I_L = I_{L_{max}} = \frac{0.7}{R_{sc}}$

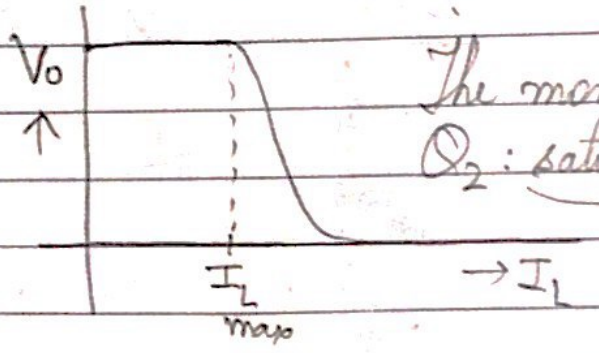
↳ This is the limit of current that can be given.

If R_L is further decreased, at this point $V_o = I_{L_{max}} \cdot R_2$

$$V_o = I_{L_{max}} \cdot R_L$$

$$\Rightarrow V_o = \left(\frac{0.7}{R_{sc}}\right) R_L$$

I_L cannot supply more than $I_{L_{max}}$.
So, as $R_L \downarrow$, V_o starts to decrease.



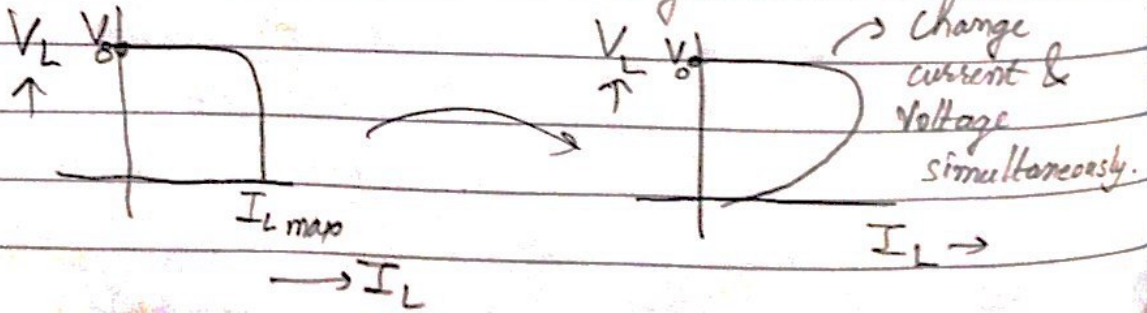
The moment $I_{L_{max}}$ is reached, Q_2 : saturated & Q_1 : off.

Why?
Q_2 : saturated
$\Rightarrow$ EB : FB, CB : FB
Base of Q_1 is RB
$\Rightarrow$ off

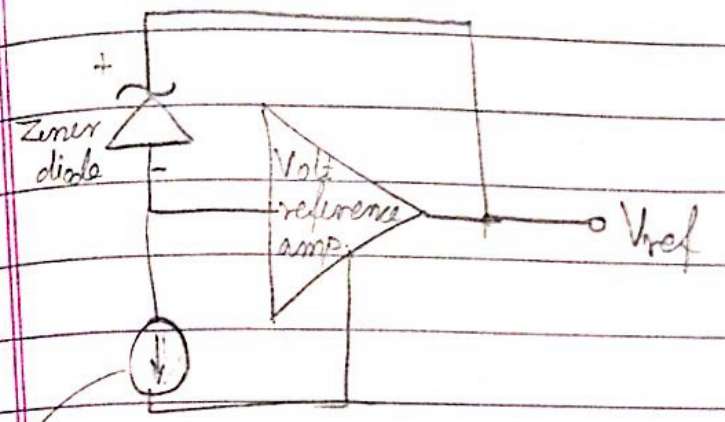
Note : $V_o \downarrow$ as $R_L \downarrow$
But current through R_L maintains at $I_{L_{max}}$.

($I_{L_{max}} = 1$ A. $\Rightarrow$
if $\frac{V_o}{R_L} = 1$A i.e $R_L = 18\,\Omega$,
This is point of saturation)

Now, say $R_L \simeq 1\,\Omega$; We are flowing 1A current through such small R_L. So, load will burn. So, current foldback circuit is used to prevent this.
i.e, make characteristics changed:



IC VOLTAGE REGULATOR (μA 723)



Q_1 & Q_2 : to limit o/p current

→ Using a constt current source makes V_Z fix at constt value.

Can operate in 2 modes : low voltage mode & high voltage mode.

Low Voltage Regulator
(V_o = 2 to 7 V)

Current limit transistor remains non conductive

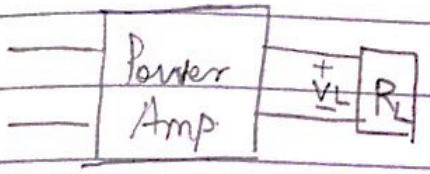
POWER AMPLIFIERS

✓ Used to deliver large power to the load at certain freq.

✓ Normally, from 0.5W to more than 10KW.

✓ $\frac{P_{out}}{P_{in}}$ → very high

✓ Voltage need not be amplified (Power is amplified)



$P_o = \frac{V_L^2}{R_L}$

↳ If $V_L = V_o \sin\omega t$

⇒ its varying with time

So, average value of power can be calculated

→ avg. value of P_o

$\langle P_o \rangle = \frac{V_o^2 \sin^2\omega t}{R_L}$

$= \frac{V_o^2 (V_2)}{R_L}$

$\Rightarrow \langle P_o \rangle = \frac{V_o^2}{2R_L}$ = Avg. power for a sinusoidal signal

Extra:

If $y(t) = y_o \sin\omega t$

$\langle y(t) \rangle = \frac{1}{2\pi} \int_0^{2\pi} y_o \sin\omega t \, dt$ (avg)

$= 0,$

↳ As true average = 0

⇒ we use RMS value.

So, $\sqrt{\langle y^2(t) \rangle} \equiv$ r.m.s

$\langle y^2(t) \rangle = \frac{1}{2\pi} \int_0^{2\pi} y_o^2 \sin^2\omega t \, dt$

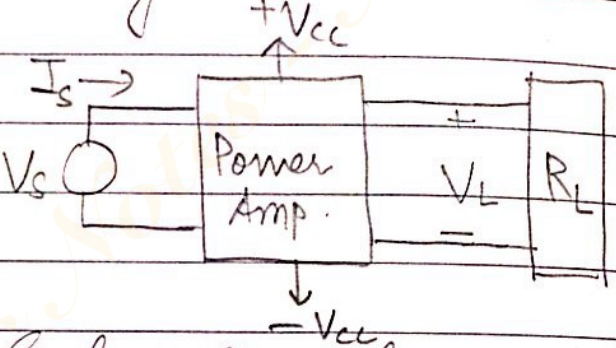
$\langle y^2(t) \rangle = \frac{y_o^2}{2}$

$\Rightarrow \sqrt{y^2(t)} = \frac{y_o}{\sqrt{2}}$ = rms value

✡ Basic Considerations

(1) • High Efficiency (η)

Any amp. has large i/p impedance.
⇒ it doesn't take large i/p current
So, i/p power is low. (negligible)
Now, amplific^n of low power to a very high power is done. This is done through batteries



So, basically, takes part of DC power & converts it to a large o/p power

$$P_{output} + P_{dissipation} = P_{input} + P_{DC}$$

P_{input} → almost negligible.

$$\Rightarrow P_{dc} = P_o + P_{diss}$$

Efficiency ⇒ P_{diss} shouldn't be there, if possible.

If $P_{dc} = P_o$, efficiency = 100%

$$\eta = \frac{P_o}{P_s}$$

P_o → o/p power.

P_s → Supplied power ≡ P_{dc}.

(2). High heat transfer or thermal conductivity.

* Note : $P_{dissipation}$ cannot be completely zero.

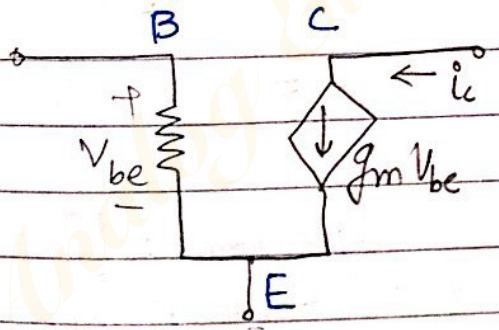
(∵ As high current flows through R_L, junction temp can ↑. To avoid it, HEAT SINKS are placed in the o/p stage)

(3)° High o/p current, low o/p impedance.

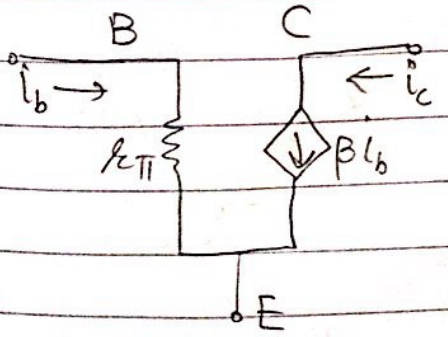
(4)° Minimum Distortion.

(5)° Large Signal Operation.

* For a BJT under SMALL SIGNAL, we can model the transistor as :-



or



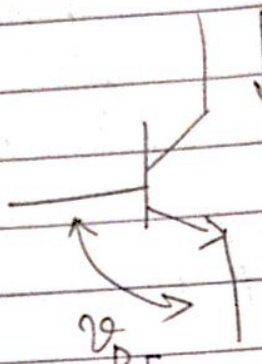
∴ Such models are NOT applicable.
(∵ ∃ large signals & high currents)

If i_c has to be large enough to supply to load, it cannot function

Good

☆ Extra

Why large signal doesn't work in such small signal models?



By junction char,

$$i_C = I_S\left[e^{\frac{v_{BE}}{V_T}} - 1\right]$$

$$\Rightarrow I_C + i_c = I_S\left[e^{\frac{v_{be}}{V_T}} \cdot e^{\frac{V_{BE}}{V_T}} - 1\right]$$

Assume $V_{BE} \simeq 0.7\,V$

& v_{be} = Signal voltage ≡ assumed very small

$$\Rightarrow V_{BE} + v_{be} \simeq 0.7$$

$$\Rightarrow I_C + i_c = I_S\left[e^{\frac{v_{be}}{V_T}} e^{\frac{V_{BE}}{V_T}}\right]$$

$$\Rightarrow I_C + i_c = I_C\left[e^{\frac{v_{be}}{V_T}}\right]$$

$$\Rightarrow i_C = I_C e^{\frac{v_{be}}{V_T}} - I_C$$

Signal collector current ←

$$\Rightarrow i_c = I_C\left[e^{\frac{v_{be}}{V_T}} - 1\right]$$

→ non linear.

Now, we supply very very small signal

i.e, $v_{be} \ll V_T$.

Now

$$e^x = 1 + x + \frac{x^2}{2} + \cdots$$

as x i.e $\frac{v_{be}}{V_T}$ is very small

$\Rightarrow x^2$ is further small & can be ignored.

So,

$$i_c = I_c\left(\frac{v_{be}}{V_T}\right)$$

$$\Rightarrow i_c = g_m(v_{be})$$

$g_m \rightarrow$ a constt

↳ So, now its linear rel^n.
(WORKABLE FOR SMALL SIGNAL)

If we use large signal,

$$i_C = I_C\left[e^{\frac{v_{be}}{V_T}} - 1\right]$$

Now, complete exponential terms have to be dealt. We cannot truncate.

So, relationship is non-linear.

Hence, $i_c = g_m v_{be}$ is no longer valid

$\Rightarrow$ We cannot use small signal models

methods

* Graphical models are used for Large Signals to solve for currents & voltages.

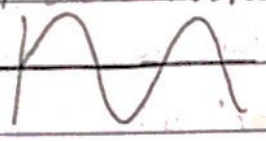
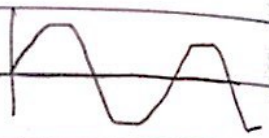
* Amplifier will suffer from distortions under large signals.

Amplifier distortion :

Amplitude → Harmonic.

Suppose i/p freq = ω_s. If we get freq components at o/p = $\omega_s, 2\omega_s, 3\omega_s$ --- So, it's harmonic distortion

∃ another case like, consider,

i/p =  . If we get o/p = 

Such a distortion is called Amplitude distortion.

* In a general case,

Signal collector current is expressed as :

* $i_c = a_1 i_b + a_2 i_b^2 + \cdots + a_n i_b^n$ ⟶ (1)

↳ ≡ non linear

→ (Note : For small signal, we had $i_c = \beta i_b$)

↳ If ∃ no distortion, $i_c = a_1 i_b$. (Distortion free)

Consider a general case.

i_b = sinusoidal signal = $I_{bm} \cos \omega t$.

$\Rightarrow i_c = a_1 I_{bm}\cos\omega t + a_2 (I_{bm}\cos\omega t)^2 + \dots$

$I_{bm}^2\cos^2\omega t = \left(\frac{\cos 2\omega t + 1}{2}\right) I_{bm}^2$

Now,

$i_c = I_c + i_c$

$= \frac{I_{bm}^2}{2} + \frac{I_{bm}^2 \cos 2\omega t}{2}$

DC term, $\cos 2\omega t$ term

$\Rightarrow i_c = I_c + (a_1 I_{bm}\cos\omega t) + \left(\frac{a_2 I_{bm}^2}{2} + \frac{a_2 I_{bm}^2}{2}\cos 2\omega t\right) + \dots$

$a_1 I_{bm} \rightarrow B_1$

$\frac{a_2 I_{bm}^2}{2} \rightarrow B_0$

$\frac{a_2 I_{bm}^2}{2} \rightarrow B_2$

$i_c = I_c + i_c = I_c + B_0 + B_1\cos\omega t + B_2\cos 2\omega t + \dots$

$I_c + B_0$: const^{tt} ; $B_1\cos\omega t$: Amplified signal ; $B_2\cos 2\omega t$: 2nd harmonic

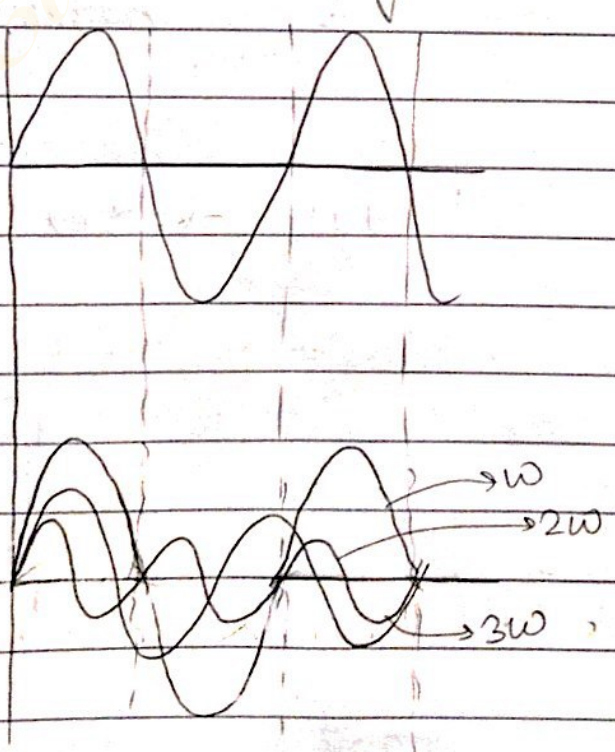
↳ ⇒ Harmonic distortion occurs.

↳ Amplitudes of harmonics

1st > 2nd > 3rd . . . .

So, 4th, 5th . . . harmonics are usually ignored

Graphically:



Harmonic Distortion is defined as

$D_2 = \frac{|B_2|}{|B_1|}$ → 2nd harmonic distortion

$D_3 = \frac{|B_3|}{|B_1|}$ → 3rd " "

$D_4 = \frac{|B_4|}{|B_1|}$ → 4th " "

. . . .

RMS of all these distortions = Total harmonic distortion (THD)

* ↳ $D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots}$

* O/p Power delivered to the load.

$P_o = I_o V_o$

$= I_o (I_o R_L)$

$\Rightarrow P_o = I_o^2 \cdot R_L$; I_o = o/p current = Signal collector current, i_c.

↳ as $i_c = I_c + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + \cdots$

Power = $P_{DC} + P_{AC} = P_o(t)$

$P_{DC} \rightarrow (I_c + B_0)^2 R_L$

P_{AC} depends on time $\rightarrow (B_1 \cos \omega t + B_2 \cos 2\omega t + \cdots)^2 R_L$

$\Rightarrow i_c$ depends on time. So, power depends on time.

Avg. Power,

$$\langle P_o(t) \rangle = \langle i_o^2(t) \rangle R_L$$

↳ Taking only fundamental freq in the beginning.

$\therefore i_o(t) = B_1 \cos \omega t$

$$\Rightarrow \langle i_o(t) \rangle = \frac{B_1}{\sqrt{2}}$$

$$\Rightarrow \langle i_o^2(t) \rangle = \frac{B_1^2}{2}$$

$$\Rightarrow \langle P_o(t) \rangle \Big|_{\text{1st harmonic}} = \frac{B_1^2}{2} R_L = P_1, \text{ say} \rightarrow (1)$$

$$\text{Hy. } \langle P_o(t) \rangle \Big|_{\text{2nd harmonic}} = \frac{B_2^2}{2} R_L$$

Total Average AC power.

$$= \langle P_o(t) \rangle = \left(B_1^2 + B_2^2 + \cdots \right) \frac{R_L}{2}$$

$$= \left(1 + \left(\frac{B_2}{B_1} \right)^2 + \left(\frac{B_3}{B_1} \right)^2 + \cdots \right) \frac{B_1^2 R_L}{2}$$

$$= \left(1 + D_2^2 + D_3^2 + \cdots \right) P_1$$

$$\approx \left(1 + D_2^2 \right) P_1$$

↳ others ignored → small

$$\Rightarrow \boxed{\langle P_o(t) \rangle = \left(1 + D^2 \right) P_1}$$

★

Puffin
Date
Page

Q Given: $i_c = 100(1+V_I) + 20(1+V_I)^2$ mA
in a power amplifier.
Determine I_{CQ} & I_{avg} in mA & percent distortion.
Given:- i/p V_I is sinusoidal, with max. value 0.5 V.

Soln :- $i_c = 100(1+V_I) + 20(1+V_I)^2$

↳ Put $V_I \Rightarrow$ AC term = 0.
we get
I_c i.e DC current = 100 + 20 = 120 mA.

Now, Given: $V_I = 0.5\cos\omega t$.

Now,
$i_c = I_c + i_c$

$\Rightarrow i_c = 100 + 100(0.5)\cos\omega t + 20\left(1 + (0.5)^2\cos^2\omega t + 2(0.5)\cos\omega t\right)$

Now, finding $\langle i_c \rangle$

↳ Avg $(\cos\omega t) = 0$

$\Rightarrow \langle i_c \rangle = 100 + 20 + \left[(0.5)^2\cos^2\omega t\right] \times 20$

↳ $\frac{1}{2} + \frac{\cos 2\omega t}{2}$

$= 100 + 20 + \left[(0.5)^2\left(\frac{1}{2}\right)\right] \times 20$ ↳ avg = 0

$= 120 + 2.5$

$\Rightarrow I_{avg} = 122.5$ mA.

Now, $D = \frac{\sqrt{B_2^2 + B_3^2 + \cdots}}{|B_1|}$

In the given expression, $B_3, B_4 \cdots = 0$.

$\Rightarrow D = \frac{|B_2|}{|B_1|} \times 100$.

$\Rightarrow D = \frac{2.5}{70} \times 100 = 3.57\%$

2.5 → coeff. of $\cos^2 \omega t$

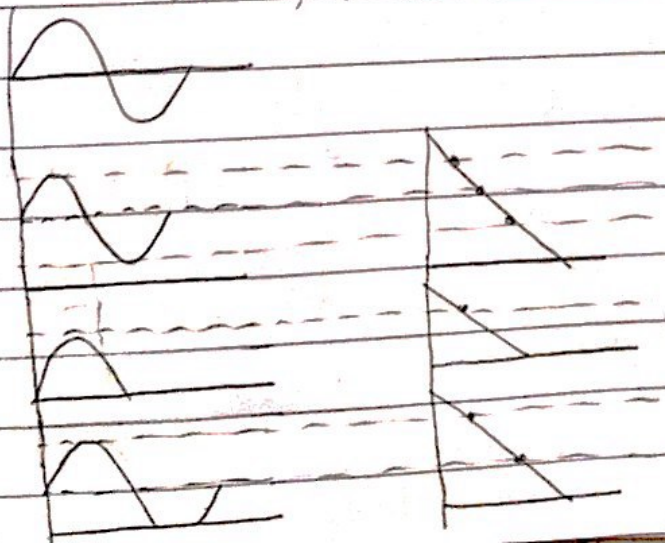
70 → coeff. of $\cos \omega t$.

CLASSIFICATION OF POWER AMPLIFIERS.

Class A : Conducting for complete cycle (1)

Class B : Conducts for half cycle. So, 2 transistors are needed for full cycle.

Class AB : At region close to cut off, both transistors are working. At region below a certain value, A works. & above a certain value, B works.



(Receiver gets the same o/p, just in different ways)

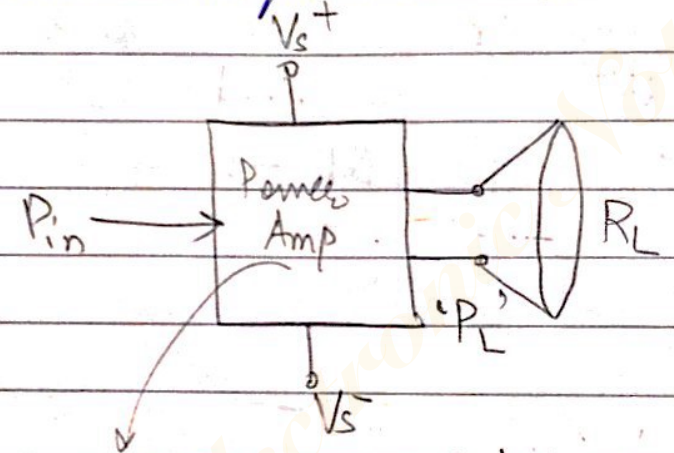
* Emitter follower ⇒ if i/p voltage = V_i, o/p voltage = V_o (same) ≡ Voltage follower

Avg. AC power across load R_L, with $v_o(t)$ & $i_o(t)$ (instantaneous voltage & current)

$$P_L = \frac{1}{T}\int_0^T i_o(t)\, v_o(t)\, dt$$

Power Conversion Efficiency : $\eta = \frac{P_L}{P_{IN}}$

Power Dissipation : $P_D = P_{IN} - P_L = P_L\left(\frac{1}{\eta} - 1\right)$



DC power converted to AC power

So, in above diagram ; by conserv^n of energy

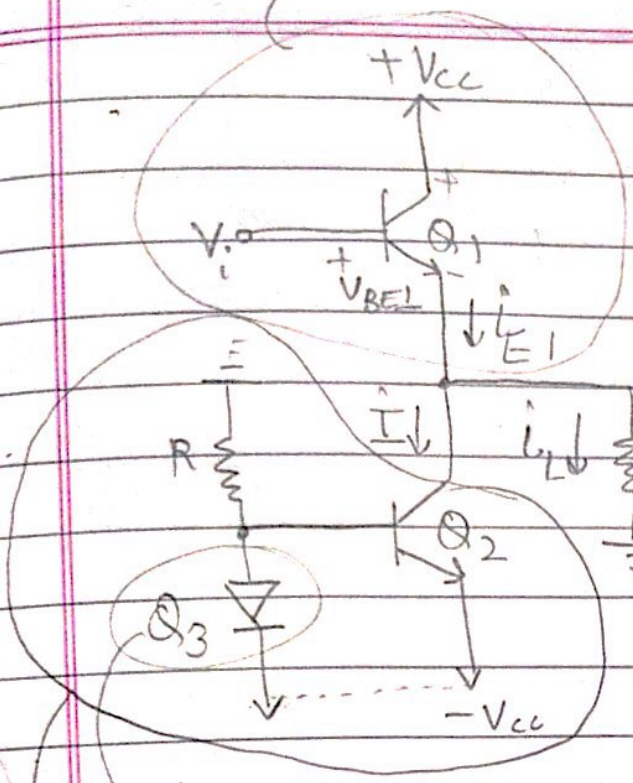
$P_{signal} + P_s = P_{Load} + P_{dissipation}$

P_{signal} : generally very small (Generally ignored)

P_s : due to V_s^+ & V_s^- = P_s^+ & P_s^-

$\Rightarrow P_s = P_L + P_D$

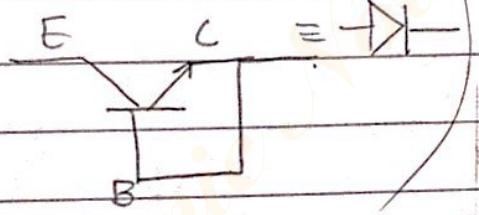
Common collector configuⁿ



From Q_3, voltage across its terminals = 0.7 (note: Q_3 is FB)

As, B & E of Q_2 also remain at a constt voltage 0.7V. So, I remains constt

It a diode connected transistor



current source.

* Power dissipated by $Q_1 = P_{D_1} = V_{CE(t)} \cdot i_{E1}$

$\Rightarrow P_{D_1} = (V_{cc} - 0)(I)$

$\Rightarrow P_{D1} = V_{cc} I$

↳ Ckt dissipates this power → drains battery

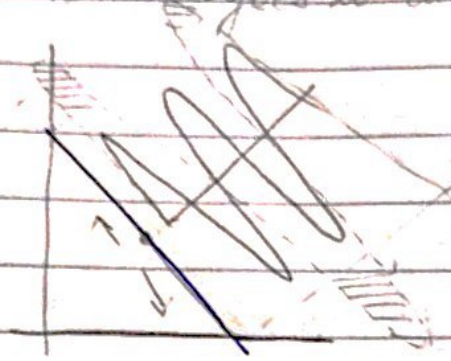
- Quiescent condⁿ: Condⁿ with no i/p. Current I flows through Q_2. Nothing goes through I_L. Here, $i_{E_1} = I$.

- As +ve value is supplied by i_{E1}, $i_{E1} \neq I$ any longer. Hence, it becomes $i_L = i_{E1} - I$.

For -ve value, $i_{E1} < I$

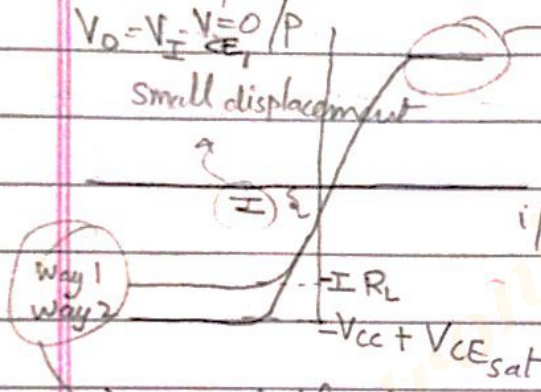
* Drawback of class A : In case of NO supply ($V_i = 0$)
But, Q_1 = power amp = ON (still not OFF). It's in Q-state. So, ∃ large power dissip^n through transistor (in standby mode)

Transistor Q1 has to be designed in such a way that when we see operating point limit, we can find when it goes to cut off or satur^n.



Class A : For transistor to be class A, it should give o/p for complete 1 cycle (atleast) without going to cut off.

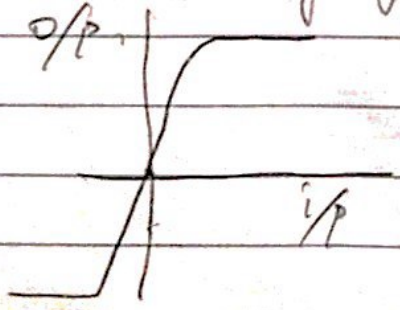
* Transfer characteristics



→ one of the two ways will be applied depending on what comes first (that is used for lower end of transfer char.)

→ satur^n
↳ can occur in 2 ways
If Q_1 goes to cut off before Q_2 goes to satur^n, limiting value of current = $-I R_L$
When Q_2 goes to satur^n, $V_{CE}|_{Q_2} = 0.2$
So, current = $(-V_{cc} + V_{CE_{sat}})$
Assume :
$I_L < V_{cc} - V_{CE_{sat}}$

For ideal voltage follower, $V_o = V_I$
↳ goes through origin.



: Ideal

Continued later

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Q(4) Design class A power amp :

$V_{cc} = \pm 15\ V$

$V_{CE}_{sat} = 0.2\ V$

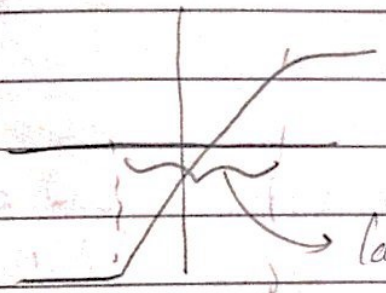
$V_{BE} = 0.7\ V$

β = very large

$R_L = 1\ k\Omega$

Find : (a) Value of R for largest possible o/p signal swing.

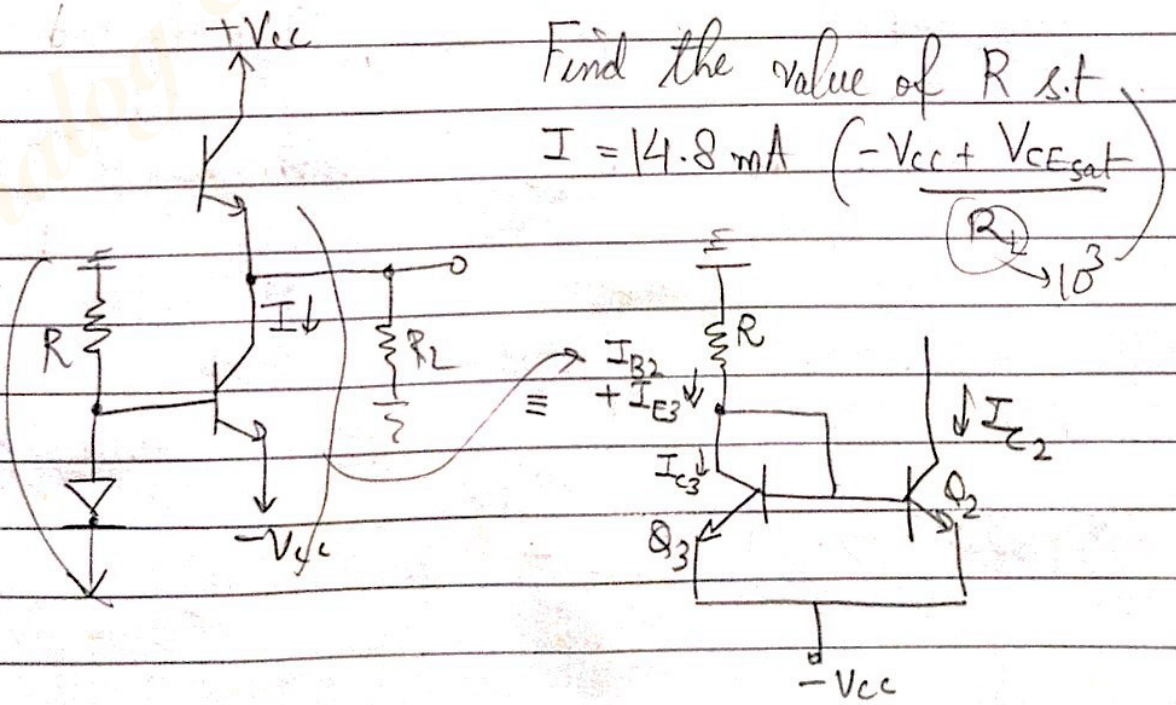
(b) R, cutting o/p signal swing & corresponding emitter current.



The largest value of I_e

$\geq -V_{cc} + V_{CE_2 sat}$.

largest possible swing of current.



Find the value of R s.t.

$I = 14.8\ mA \left(\frac{-V_{cc} + V_{CE_{sat}}}{R_L \to 10^3}\right)$

From previous fig,

$I_R = I_{C3} + I_{B3} + I_{B2}$

$= I_{E3} + I_{B2}$

As emitter for both transistors is connected, & if $Q_2 = Q_3$, then,

$I_{C3} = I_{C2}$

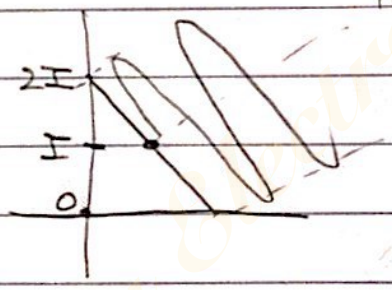
Considering $I_{B3} \simeq 0$

$\Rightarrow I_{C3} = I_{E3}$

$\Rightarrow I_R = I_{C3} + I_{B2}$

Now, $R \leq \frac{V_R}{I_R} = \frac{0 - 0.7 - (-15)}{14.8} \simeq 0.97 k\Omega$

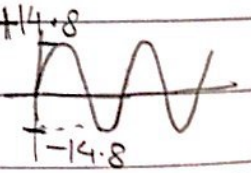
(b) Max. condⁿ: I goes through Q_2 & I goes through R_L $\Rightarrow$ 2I is supplied from $+V_{cc}$



$V_{o_{min}} = (-V_{cc} + 0.2) = -14.8$

$V_{o_{max}} = +V_{cc} + V_{CE_2}{}_{sat} = +14.8$

When $V_o = V_{o_{max}}$ $\rightarrow$ A sinusoid



$i_{E_1} = I + i_L = 14.8 + \frac{14.8}{1K\Omega} = 29.6 mA$

When $V_o = V_{o_{min}}$

$i_{E_1} = I - i_L = 14.8 - \frac{14.8}{1k\Omega} = 0 mA$

* Power Dissipation in Q_1

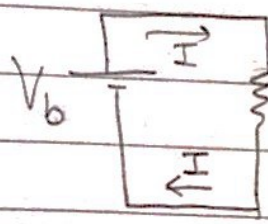
Instantaneous power dissip^n in Q1 :

$$P_{D1} = V_{CE_1} i_{C_1}$$

$$P_{D1} = (V_{CC} - V_o) \times \left(I + \frac{V_o}{R_L}\right)$$

$$\Rightarrow P_{D1} = V_{CC} I + \left(\frac{V_{CC}}{R_L} - I\right) V_o - \frac{V_o^2}{R_L}$$

Consider :



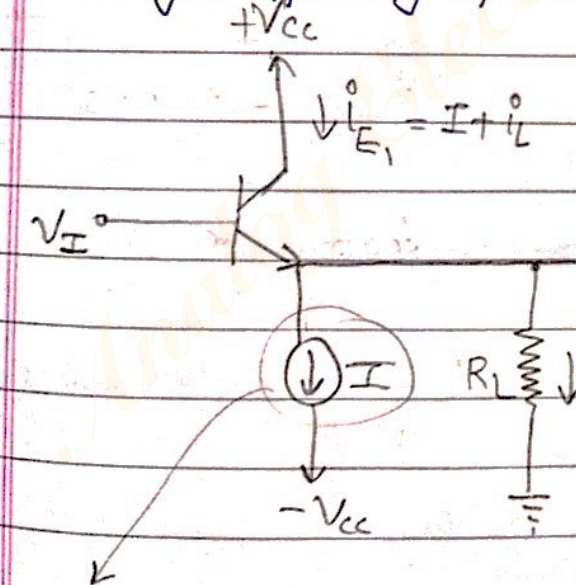
$$P_b(t) = (V_b)(I_b(t))$$

V_b → fixed

$I_b(t)$ → sometimes taken more, sometimes less by circuit

* Finding efficiency of Class A Power amplifier :

Consider the following circuit.



current mirror simplified to a constt. current

Clearly, $i_{E_1} = I + i_L$

& $i_L = \frac{v_o}{R_L} = \frac{V_o}{R_L} \sin\omega t$

$\frac{V_o}{R_L} \rightarrow I_o$

Note: Max. value of $i_L = I$

$\because i_L$ should be $I\sin\omega t$.

As $i_{E_1} = I + i_L$,

we cannot take i_{E_1} below 0. So, $i_{E_1 min} = 0$ (cut off of transistor)

$\Rightarrow I + i_L = 0$

$\Rightarrow i_L = \text{sinusoid} = I\sin\omega t$

In general, $i_L = I_0 \sin\omega t$

(generally, we keep $I_0 < I$ supplied by current source)

Now, Supplied power $= \pm V_{cc}$

& $\langle P_s^+ \rangle = ?$ (Avg. power supplied by +ve battery)

Now, Instantaneous $P_s^+ = V_{inst} \times I_{inst}$

$= V_{cc} \times i_{E_1}(t)$

V_{cc} → no change

$\Rightarrow$ Instantaneous $P_s^+ = V_{cc} \times (I + i_L(t))$

$= V_{cc} \times (I + I_0 \sin\omega t)$

$= V_{cc} \times \left(I + \frac{V_0}{R_L} \sin\omega t\right)$

$\Rightarrow$ Instantaneous $P_s^+ = V_{cc} I + V_{cc} \frac{V_0}{R_L} \sin\omega t$

$\Rightarrow$ Avg $P_s^+ = \langle P_s^+ \rangle = \left\langle V_{cc} I + V_{cc} \frac{V_0}{R_L} \sin\omega t \right\rangle$

$= \langle V_{cc} I \rangle + \left\langle V_{cc} \frac{V_0}{R_L} \sin\omega t \right\rangle$

$= V_{cc} I + V_{cc} \frac{V_0}{R_L} \underbrace{\langle \sin\omega t \rangle}_{0}$

$\Rightarrow \langle P_s^+ \rangle = V_{cc} I$

Now,

$\langle P_s^- \rangle = ?$

P_s^- = Instantaneous $P_s^- = V_{cc} I$.

$\Rightarrow \langle P_s^- \rangle = V_{cc} I$.

$\Rightarrow \langle P_s \rangle = \langle P_s^+ \rangle + \langle P_s^- \rangle$

$\Rightarrow \langle P_s \rangle = 2 V_{cc} I$

o/p (load) $\langle P_L \rangle$; dissipation (heat) $\langle P_D \rangle$

Now, $P_L(t) = (\text{Instt } V_o)(\text{Instt } I_o)$

$= i_L(t)\, V_L(t)$

$= (I_o \sin\omega t)(V_o \sin\omega t)$

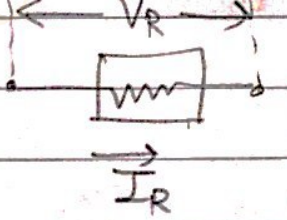
$\Rightarrow P_L(t) = \frac{V_o^2}{R_L} \sin^2\omega t$

$\Rightarrow \langle P_L \rangle = \frac{V_o^2}{R_L} \langle \sin^2\omega t \rangle$, $\langle \sin^2\omega t \rangle \to 1/2$

$\Rightarrow \langle P_L \rangle = \frac{V_o^2}{2R_L}$

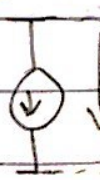
Now, power is dissipated across transistor (P_{D_1}) & current mirror (P_{D_2}); Now $P_{D_2} = ?$ & $P_{D_1} = ?$

Idea:



$\Rightarrow P_R = V_R I_R$

So,

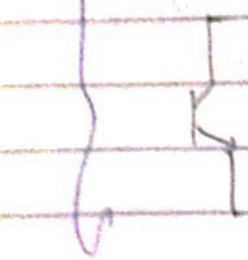


$\Rightarrow P_{D_2}(t) = [V_o - (-V_{cc})] I$

$= (V_o + V_{cc}) I$

$\Rightarrow P_{D_2}(t) = (V_o \sin\omega t + V_{cc}) I$

$\Rightarrow \langle P_{D_2} \rangle = V_{cc} I$



$$\Rightarrow P_{D_1}(t) = (V_{cc} - V_o)\, i_{E_1}(t)$$

$$= (V_{cc} - V_o \sin\omega t)(i_L(t) + I)$$

$$= (V_{cc} - V_o \sin\omega t)(i_L \sin\omega t + I)$$

$$\Rightarrow P_{D_1}(t) = \left(V_{cc} - V_o \sin\omega t\right)\left(\frac{V_o}{R}\sin\omega t + I\right)$$

$$\Rightarrow \langle P_{D_1} \rangle = \left\langle \left(V_{cc} - V_o \sin\omega t\right)\left(\frac{V_o}{R}\sin\omega t + I\right) \right\rangle$$

$$= \left\langle \frac{V_{cc} V_o}{R}\sin\omega t + V_{cc} I - \frac{V_o^2}{R}\sin^2\omega t - V_o I \sin\omega t \right\rangle$$

$$\Rightarrow \langle P_{D_1} \rangle = 0 + V_{cc} I - \frac{V_o^2}{R}\left(\frac{1}{2}\right) - 0$$

$$\Rightarrow \langle P_{D_1} \rangle = V_{cc} I - \frac{V_o^2}{2R}$$

$$\Rightarrow \langle P_D \rangle = \langle P_{D_1} \rangle + \langle P_{D_2} \rangle$$

$$= V_{cc} I - \frac{V_o^2}{2R} + V_{cc} I$$

$$\langle P_D \rangle = 2V_{cc} I - \frac{V_o^2}{2R}$$

Checking: We should get

$$\langle P_S \rangle = \langle P_D \rangle + \langle P_L \rangle$$

$$\Rightarrow 2V_{cc} I = 2V_{cc} I - \frac{V_o^2}{2R} + \frac{V_o^2}{2R}$$

$$\Rightarrow 2V_{cc} I = 2V_{cc} I.$$

So, satisfied.

Note: We use P_L to drive a load.
$\Rightarrow \langle P_L \rangle$ = useful power.
& we use P_S to give supply
$\Rightarrow \langle P_S \rangle$ = supplied power.

So, efficiency, $\eta = \dfrac{\langle P_L \rangle}{\langle P_S \rangle}$

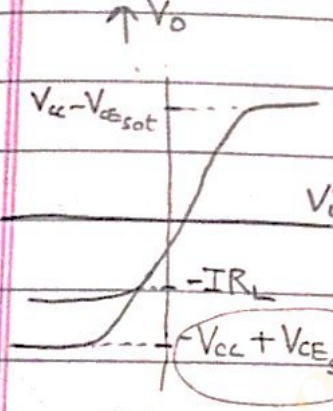
$$= \frac{V_0^2/2R_L}{2V_{CC}I}$$

$$\Rightarrow \eta = \frac{V_0^2}{4V_{CC}IR_L}$$

↳ V_0: peak value of voltage across load

∀ practical purposes, $V_0|_{max} = V_{CC}$.

(Ignoring drop due to $V_{CE} = 0.2V$)



Also, under limiting cond^n, $(IR_L) \approx V_{cc}$

(Actually, $IR_L > V_{cc}$)

$$\Rightarrow \eta = \frac{(V_{cc})^2}{4(V_{cc})(V_{cc})}$$

$\Rightarrow \eta = 25\%$

↳ max efficiency of class A amp.

Q.(A) Continued...

If amp. is designed for a 10V peak sinusoid o/p voltage, what is power conversion efficiency?

* Class A : Only one transistor used to take i/p signal & supply power at o/p. So, this transistor should be ON for entire duration of i/p signal

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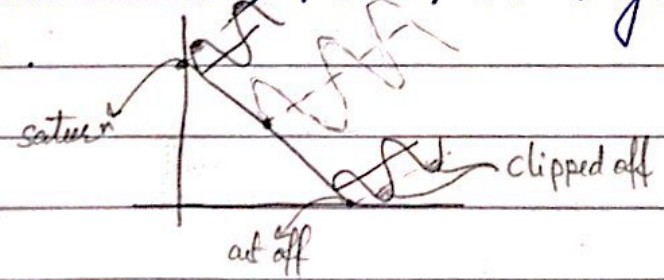
Sol^{n} :- $(V_o)_{max} = 14.8$

$$\eta = \frac{P_L}{P_S} = \frac{1}{4}\frac{\langle V_o \rangle^2}{I R_L V_{cc}} = \frac{10^2}{4 \times 14.8 \times 1 \times 15} = 11.3\%$$

* Disadvantages of Class A
  - ↳ low efficiency
  - ↳ unnecessary power drainage (through Q1)
* Advantage
  - ↳ Very good quality o/p : Low distortion.
    - ↳ works on linear region of transfer char. ⇒ sinusoidal i/p gives sinusoidal o/p (pure).
  - ↳ used for low power circuit.

Basic problem in Class A is that I'm supposed to choose an operating pt. in the middle.
If we choose a region near cut off or satur^{n}, we wont have excess power drainage (when Amp. not in use), but, the signal distortion comes.

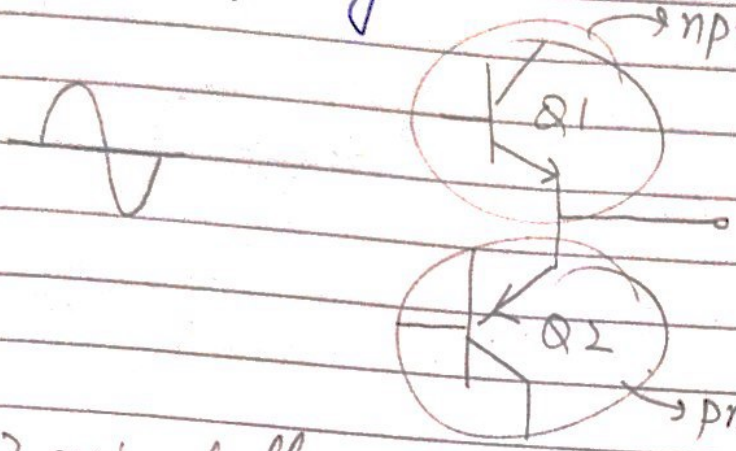


Note : Class A has only a single power transistor (Q1). Other transistor (Q2) is just a current mirror circuit (to bias).

✱ CLASS B

both emitter followers

Alternative : Use two transistors to share the i/p signal.

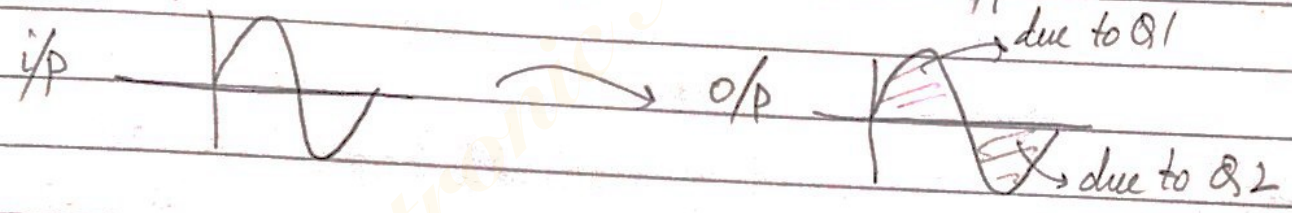


Same signal is presented to both transistors.

Q1, Q2 are in cut off region.

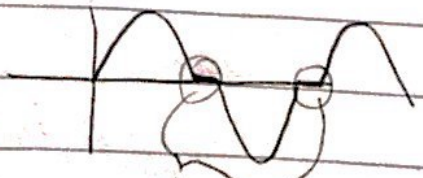
For a +ve voltage, Q1 is on (npn) & Q1 gives current at o/p, but Q2 is off → base

For -ve voltage supply, Q2 is on (pnp), & it gives current at o/p, but Q1 is off.



Advantage : Quiscent power drain = 0.
So, high efficiency comes (≃ 78 %)

Disadvantage : Notice that when Q1 is on, Q2 remains off. As soon as Q1 gets off, Q2 gets on. But, there can exist delay. This will lead to o/p like :-

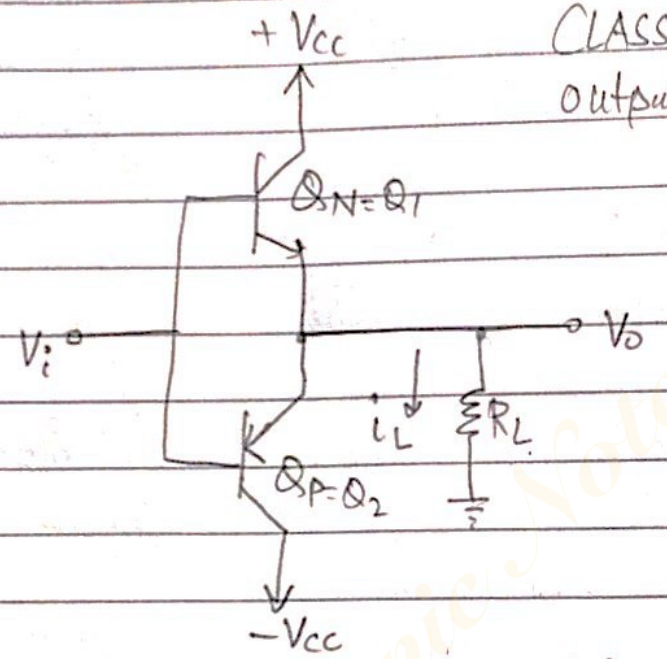


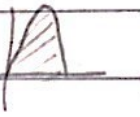
CROSSOVER ≡ Distortion

(when the cut in voltage req'd to start the transistor is not reached)

change over is not immediate.

If I'm operating in cut-off region, I need some voltage to come to active region. Due to this voltage requirement, during crossover (from +ve to -ve cycle), both transistors go through a DEAD ZONE (no o/p region). Hence, distortion comes.

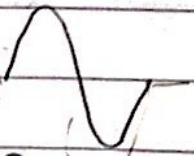


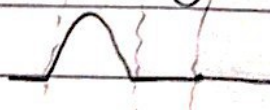
For +ve half cycle of i/p  , Q1 = on, Q2 = off. (comes from $+V_{cc}$ ⇒ +ve)

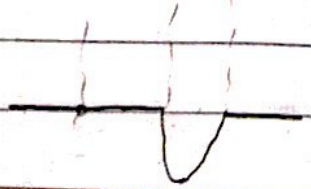
$\Rightarrow i_L = I_{EQ_1}$ & $V_o = V_i$

-ve half cycle of i/p:  , Q1 = off, Q2 = on

$i_L = I_{EQ_2}$ & $V_o = V_i$ (comes to $-V_{cc}$. So, -ve)

So, actually, if i/p = 

Current from Q1 = 

Current from Q2 = 

Case ① $V_I = 0 \Rightarrow i/p = 0$.

$\Rightarrow Q1, Q2$ = cut off

$\Rightarrow V_o = 0$.

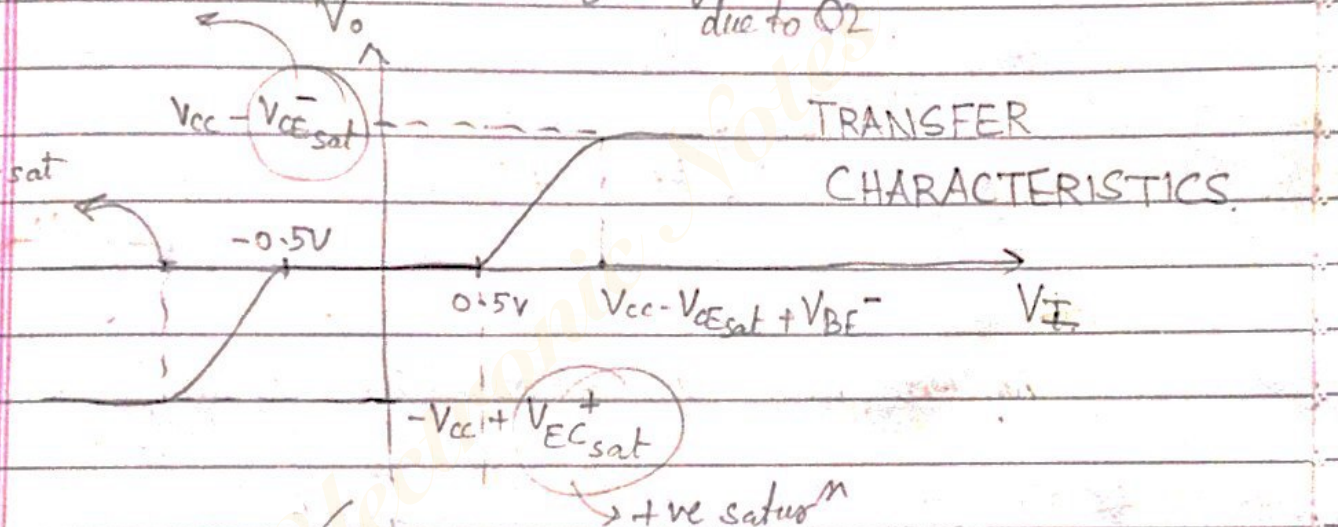
Case ② :- $V_I > 0.5$ ⇒ cut in voltage needed for transistors to operate has exceeded.

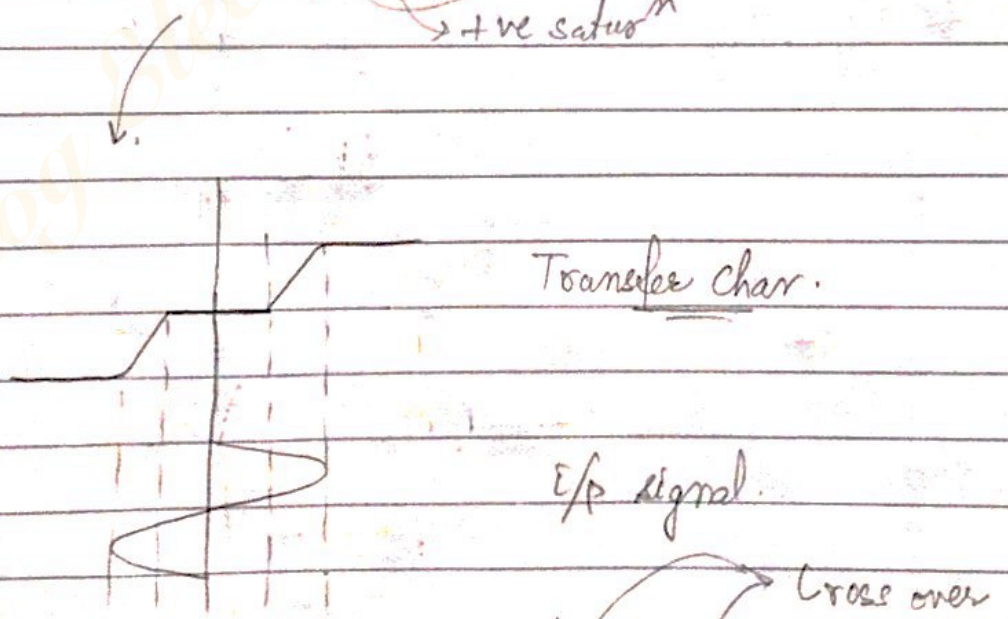
So, Q1 works.

$\Rightarrow V_o = V_{\text{due to } Q1}$

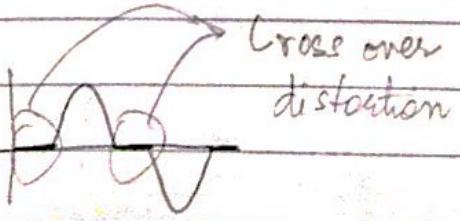
Case ③ :- $V_I < 0.5 \rightarrow Q2$ works

$\Rightarrow V_o = V_{\text{due to } Q2}$





So, we get an o/p as :-



Note : ∵ Transfer Char are non linear, ∴ I don't get i/p = o/p

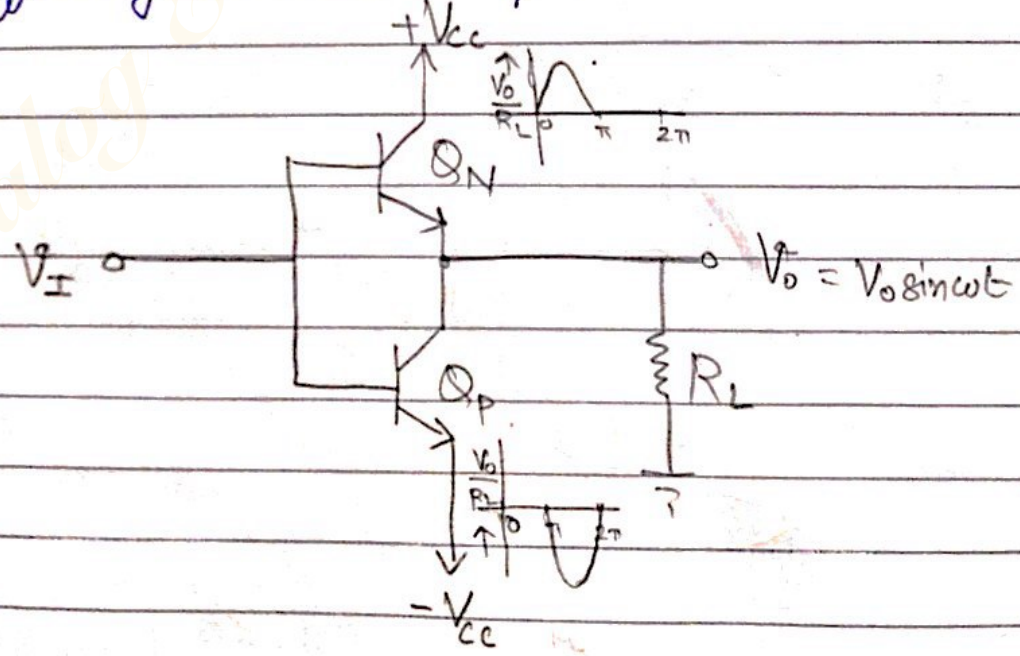
* Class B has a MAJOR problem of Crossover distortion.

* Advantage of Class B :-
  No i/p ⇒ No power drain. So, entire i/p is nearly used as o/p.
  So, power conversion efficiency is very high ($\simeq 78.5\%$ i.e $\frac{\pi}{4}$)

* In Class B, no DC cond^n is req^d ∵ Q1, Q2 are in cut off.
* In Class A, DC cond^n was req^d ∵ operating pt had to be in the middle

* Disadvantage :
  We don't get a pure sine wave.

* Efficiency Calculation for Class B.



We take avg power delivered to load $= \langle P_L \rangle$.

Now, supply power $\Big|_{avg} = \langle P_s \rangle = \langle P_s^+ \rangle + \langle P_s^- \rangle$.

dissipated power $\Big|_{avg} = \langle P_D \rangle = \langle P_{D_{QN}} \rangle + \langle P_{D_{QP}} \rangle$.

Efficiency, $\eta = \dfrac{\langle P_L \rangle}{\langle P_s \rangle}$

$\hookrightarrow \simeq 78.5\%$.

end of course